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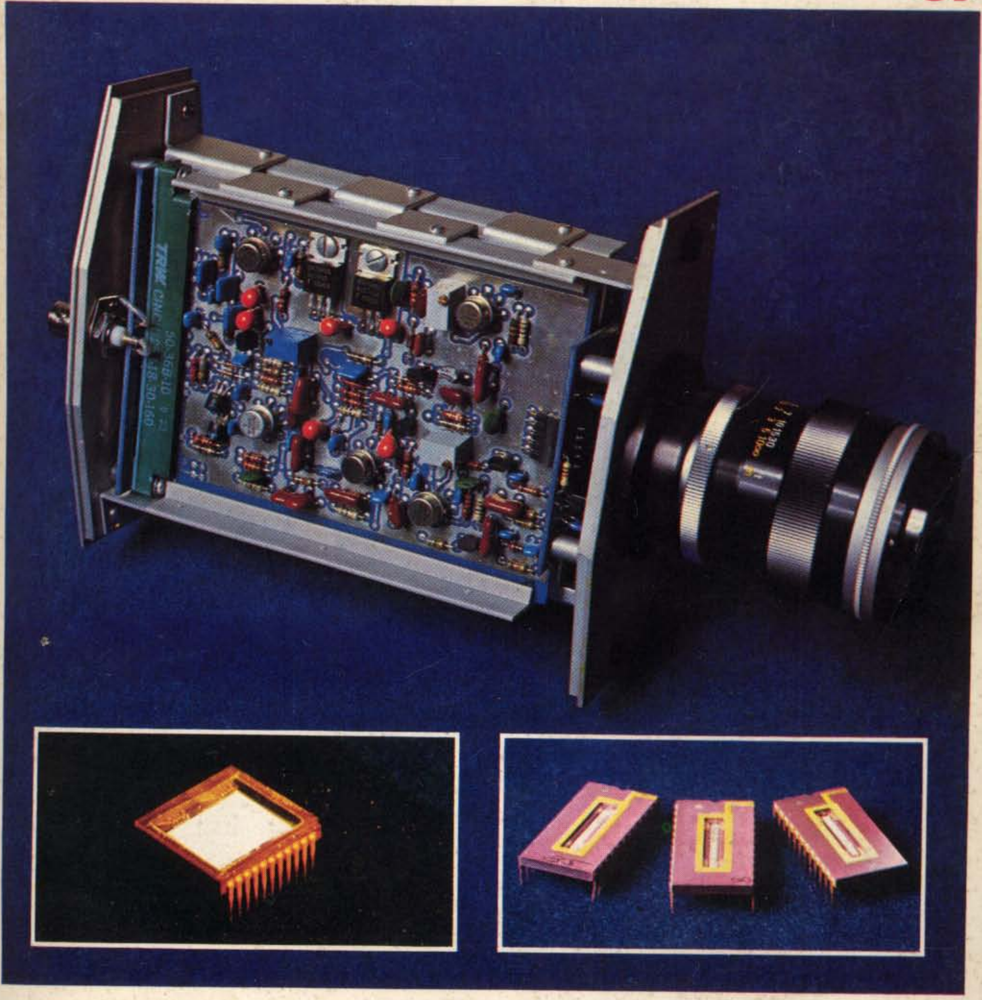
CCD

The Solid State Imaging Technology



FAIRCHILD Camera & Instrument (UK) Ltd.
230 High Street, Potters Bar, Hertfordshire EN6 5BU England
Tel: Potters Bar (0707) 51111, Telex: 262835

FAIRCHILD CHARGE COUPLED DEVICE · CCD

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Charge coupled area image sensor

Fairchild Camera and Instrument Corporation has announced what is said to be 'the world's first commercially available charge coupled area image sensor'.

The device, the CCD-201, uses an array of 100 × 100 solid state elements to create a television picture signal directly from light focused on the surface of the sensor.

The sensor is based on a new semiconductor technology called charge coupling which utilises electrical charges to collect, store and transfer information through small chips of silicon. Compared to other image sensors, CCD's are extremely sensitive to light and less subject to electrical noise and other effects that degrade signals.

The CCD-201 operates from 20V compared with the 2kV of typical vacuum tube image sensors. Nominal power consumption is 50mW.

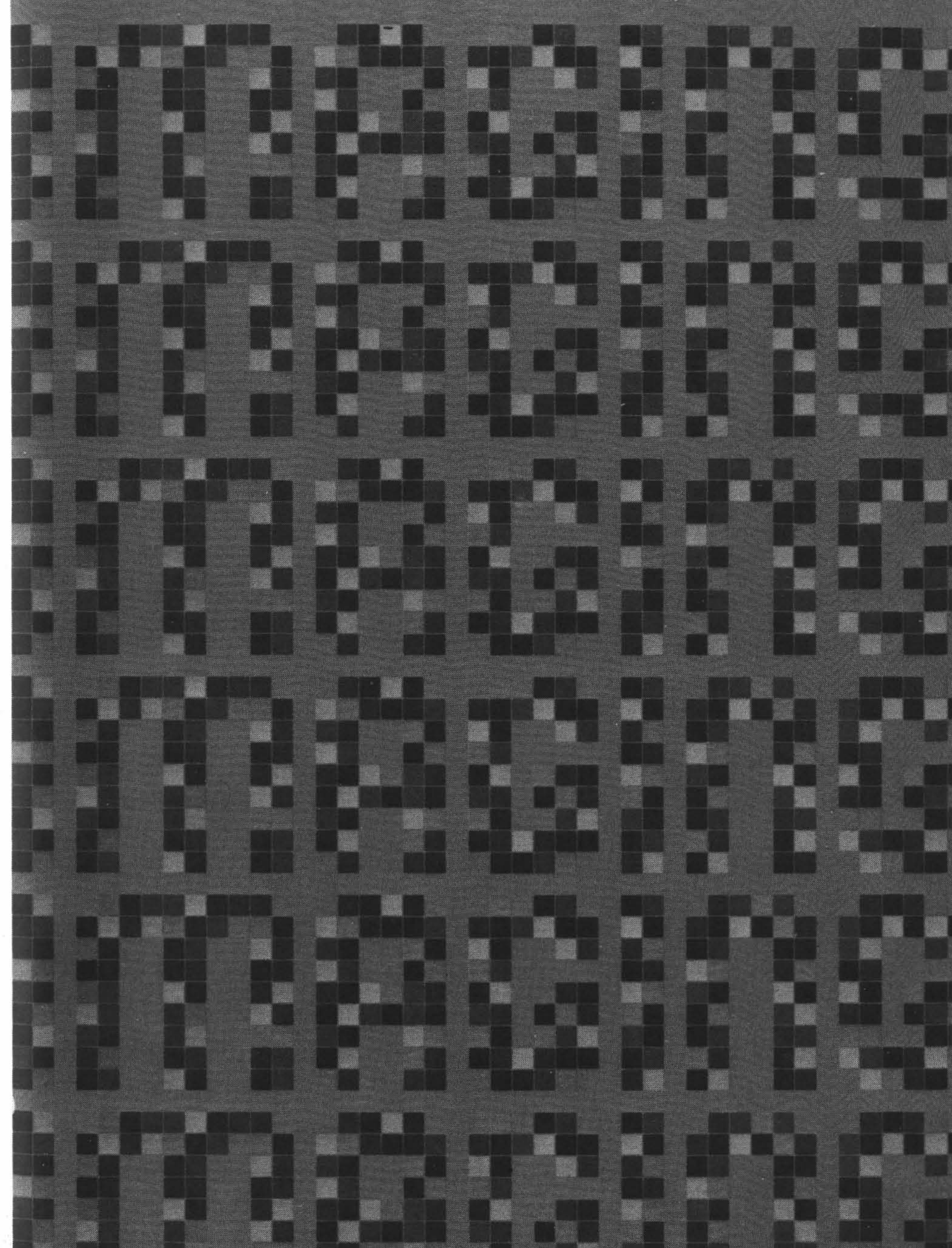
The array of light sensitive elements is arranged in 100 columns of 100 elements, with each element measuring 1·2 × 0·8mil. These columns are spaced 1·6mil apart horizontally and 1·2mil apart vertically to create the standard 3 × 4 aspect ratio. Inherent spatial accuracy of the device is 1 part in 10 000.

The device is in a 24 lead DIP measuring 0·5 × 1·25in.

22 NOV 1973

CCD IMAGING AND SIGNAL PROCESSING

Product Catalog



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Introduction

Line Scan Image Sensors

Basically, a line scan image sensor is composed of a row of image sensing elements (photosites), two analog transport registers, and an output amplifier. Light energy falls on the photosites and generates charge packets proportional to the light intensity. These charge packets are then transferred in parallel to two analog transport registers, which are clocked by 2-phase clocks. The packets are next delivered to an on-chip output amplifier where they are converted to proportional voltage levels. A series of pulses, amplitude modulated with the optical information, appear at the output.

The following tables summarize the features of Fairchild's Line Scan Imaging Products. The CCD122, CCD133, CCD142, and CCD143 are second generation image sensors which include additional integrated CCD and MOS circuitry for generation and amplification of clock signals, generation of white and black reference levels for the video output signal, generation of an end-of-scan output, and a video sample-and-hold circuit.

Key advantages of Fairchild CCD line scan sensors, due to Fairchild's Isoplanar buried-channel structure, include high data rates, high charge transfer efficiencies, low noise, and relatively small die sizes.

Line scan sensors find applications ranging from optical character recognition (OCR) using the 256 x 1 device to high speed facsimile sensing using the 1728 x 1 or 2048 x 1. The precise location of the photosites on the sensor allows the device to be used in high precision non-contact measurement applications such as dimensional measurements of objects, shape recognition and sorting, and defect detection. The line scan sensors have the same sensing element center-to-center spacing; selection is determined by the user's resolution requirement.

*ADC 53-33
*BDC 99-45

Ordering Code	Number of Elements	Element Size – Microns	Maximum Data Rate	Dynamic Range (Typical)	Responsivity (Typical)
CCD111DC	256x1	13x17	10MHz	2500:1	0.5V per μj/cm²
CCD133DC	1024x1	13x13	20MHz	2500:1	3.0V per μj/cm²
CCD121HC	1728x1	13x17	10MHz	2500:1	0.5V per μj/cm²
CCD122DC	1728x1	13x13	2MHz	2500:1	3.5V per μj/cm²
CCD142DC	2048x1	13x13	2MHz	2500:1	3.5V per μj/cm²
CCD143DC	2048x1	13x13	20MHz	2500:1	3.0V per μj/cm²

*
357.80
533.30
642.60

Line Scan Sensors

Ordering Code	Sensor Supported	Comments
CCD111DB	CCD111DC	Fairchild offers a series of printed circuit boards for use as construction aids for experimental systems using CCD line scan image sensors. These design and development boards are fully assembled and tested, and require only power supplies and an oscilloscope to display the video information corresponding to the image positioned in front of the sensor.
CCD133DB	CCD133DC	
CCD121HB	CCD121HC	
CCD122DB	CCD122DC	
CCD142DB	CCD142DC	
CCD143DB	CCD143DC	

Line Scan Design Aids
(Do not include Sensors)

Ordering Code	Number of Elements	Line Scan Rate	Exposure Time	Data Rate
CCD1100C	256x1	60Hz-35kHz	30μs-16ms	100kHz-10MHz
CCD1200C	512x1	60Hz-20kHz	51μs-16ms	100kHz-10MHz
CCD1300C	1024x1	60Hz-10kHz	102μs-16ms	100kHz-10MHz
CCD1400C	1728x1	60Hz- 6kHz	175μs-16ms	100kHz-10MHz
CCD1500C	2048x1	60Hz- 5kHz	204μs-16ms	100kHz-10MHz

Line Scan Camera Subsystems
(Include Camera, Control Unit and Interconnect Cables. Order Lens separately.)
Camera only may be ordered.

Ordering Code	Number of Elements	Grade	Dynamic Range (Typical)	Responsivity (Typical)	Maximum Frame Rate
CD211ADC	244x190	A	1000:1	5V per μj/cm²	240/s
CD211BDC	244x190	B	1000:1	5V per μj/cm²	240/s
CD211CDC	244x190	C	1000:1	5V per μj/cm²	240/s
*CD221ADC	488x380	A	1000:1	5V per μj/cm²	60/s
*CD221BDC	488x380	B	1000:1	5V per μj/cm²	60/s

Area Sensors
*NTSC Compatible

Ordering Code	Number of Elements	Maximum Frame Rate	Comment
CCD2000C	488x380	60Hz	Full NTSC Resolution
CCD2100C	244x190	240Hz	1/4 NTSC Resolution

Area Camera Subsystems
(Include Camera, Control Unit and Interconnect Cables. Order Lens separately.)
Camera only may be ordered.

Area Image Sensors

Area arrays are similar to the line scan sensors except that the photosites are arranged in a matrix format and the opaque transport registers are located between the photosite columns. The charge packets are transferred to the output amplifier in two separate fields, line by line. This technique is called the interline transfer approach.

The preceding tables summarize the features of Fairchild's Area Imaging Products. The CCD221, 488 x 380 element sensor, when operated at a 7.16 MHz horizontal clock frequency, provides a video output signal which is compatible with NTSC black and white television standards. The CCD211, 244 x 190 element sensor can fill 25% of the area of a standard television monitor with NTSC resolution imagery or it can be used with a non-standard television CRT display.

The highly precise location of the photosites allows precise identification of each component of the image signal, an important feature for applications requiring exact dimensional measurements. The devices are also well suited for use in video cameras that require low power, small size, high sensitivity and high reliability.

Camera Subsystems

Fairchild CCD camera subsystems are fully assembled and calibrated electro-optical instruments useful in a wide variety of scientific and industrial applications.

Each subsystem is comprised of a camera, a line-powered control unit, and interconnecting cables. The camera, which may be ordered separately, may be equipped with a lens suitable for the application.

Line Scan Camera resolutions of 256, 512, 1024, 1728 and 2048 elements per line are available. Line scan subsystems are particularly useful for acquisition of optical data for objects in motion, i.e., facsimile scanning of documents transported past the camera's field of view or measurement of objects carried past a camera inspection station on a conveyor belt. Typical subsystem applications include microfiche and microfilm scanning, document scanning for mark sensing, facsimile transduction and OCR data acquisition; precision non-contact measurement and inspection, flaw detection, shape analysis, dimensional measurement, color sorting; and for a wide variety of laboratory uses.

Area Camera resolutions of 244 x 190 elements and 488 x 380 elements per frame are offered. Additionally, a variety of optional accessories for use with the area subsystems are available.

Area scan subsystems are useful for acquisition of complete two-dimensional gray scale images of viewed objects. The CCD2000, when operating at a 7.16 MHz video data rate, is fully compatible with NTSC black and white television standards.

In addition to their obvious applications for television-type cameras, the area camera subsystems can be used for laboratory and industrial applications where two-dimensional image sensing is advantageous. Example applications include surveillance systems with MTI, industrial inspection in hostile environments, laser beam location and robotics.

Ordering Code	For Use With	Description
LENS13C	All	13 mm Lens, Standard C Mount
LENS25C	All	25 mm Lens, Standard C Mount
LENS50C	All	50 mm Lens, Standard C Mount
LENS75C	All	75 mm Lens, Standard C Mount
CNTRLINE	Line Scan Cameras	Control Unit with Interconnect Cables
CNTRAREA	Area Cameras	Control Unit with Interconnect Cables
CABLE	All	Interconnect Cables Only
PIX1100	CCD1100C	Pixel Locator
PIX1200	CCD1200C	Pixel Locator
PIX1300	CCD1300C	Pixel Locator
PIX1400	CCD1400C	Pixel Locator
PIX1500	CCD1500C	Pixel Locator
PIX2000	CCD2000C	Pixel Locator
PIX2100	CCD2100C	Pixel Locator
REMOKIT	Area Cameras	Remote Sensor Kit
ADDBUFF	Area Cameras	Address Buffer Board
SWEEP	Area Cameras	Sweep Generator Board
MONITOR	CCD2000C	NTSC Monitor, Black and White
211KIT	CCD2000C	Conversion Kit
221KIT	CCD2100C	Conversion Kit

Camera Accessories

Signal Processing

The capability to manipulate information in the form of discrete charge packets makes CCD technology ideal for analog signal processing. Fairchild signal processing components are monolithic silicon structures comprised of CCD analog shift registers, charge injection ports, and output charge-sensing amplifiers. They can be advantageously used for delay and temporary storage of analog video signals. The time delay for data transit through the CCD register is precisely controlled by the frequency of the externally supplied transport clock signal. Fairchild signal processing components include a sample-and-hold signal output stage for ease of application.

Fairchild video delay modules are printed circuit board structures which include the CCD321A2 device and are sold as fully assembled and calibrated units. The module is equipped for use as a variable delay circuit, using either an externally supplied or internal variable frequency clock, or for temporary analog data storage in a stopped-clock mode.

Typical applications for the CCD signal processing components and modules include time base correction for video tape recorders, fast input-slow output data expansion systems for A-D converter systems, comb filter realizations, drop-out compensators, and other analog applications up to frequencies of 30 MHz data rate.

Ordering Code	Description
CCD321A1	Broadcast Video Delay Line
CCD321A2	Industrial Video Delay Line
CCD321A3	Time Base Video Delay Line
CCD321A4	Audio Delay Line
CCD321VM	Video Module, Includes the CCD321A2 Device

Signal Processing Products

During the 70's Fairchild led the development of CCD Technology. Since the beginning, the buried-channel concept has been utilized in all CCD products. The product line therefore exhibits all the advantages of buried-channel technology including low noise, high speed and high density.

Transferring this process from an R & D to a volume production environment required extensive efforts in research, design, development and production engineering. Fairchild is the CCD industry leader.

The effort is still continuing... The 2048 x 1 is the <u>longest</u> device ever manufactured in high volume, the 488 x 380 is the <u>largest</u> chip on the market, and the CCD321 delay line is the <u>fastest</u>.

At Fairchild, CCD products are not an R & D curiosity or products looking for applications. They are here today and here to stay. The 1980's is the CCD Decade... call FAIRCHILD.

For further information on Fairchild CCD Imaging and Signal Processing products, call your nearest Fairchild Sales Office, representative or distributor.

For technical or applications information and assistance, call (415) 493-8001, (TWX 910-373-1227) or write Fairchild CCD Imaging, 4001 Miranda Avenue, Palo Alto, California 94304.

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CCD 111
256-Element Line Scan Image Sensor

CCD Imaging

Description

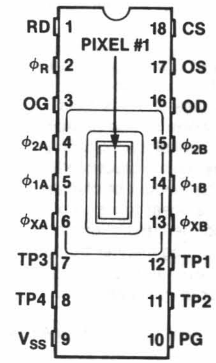
The CCD111 is a monolithic 256-element line image sensor. The device is designed for optical character recognition and other imaging applications that require high sensitivity and high speed. The CCD111 is pin-for-pin compatible with and a functional replacement for the CCD110F.

In addition to a line of 256 sensing elements, the CCD111 chip includes: two charge transfer gates, two 2-phase analog transport shift registers, an output charge detector/amplifier, and a compensation amplifier. The transport registers both feed the input of the charge detector resulting in sequential reading of the 256 sensing elements.

The cell size is 13 μm (0.51 mils) by 17 μm (0.67 mils) on 13 μm (0.51 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

- **DYNAMIC RANGE TYPICAL: 2500:1**
- **ON-CHIP VIDEO AND COMPENSATION AMPLIFIERS**
- **LOW POWER REQUIREMENTS**
- **ALL OPERATING VOLTAGES 15V AND UNDER**
- **LOW NOISE EQUIVALENT EXPOSURE**
- **DIMENSIONALLY PRECISE PHOTOSITE SPACING**

Connection Diagram

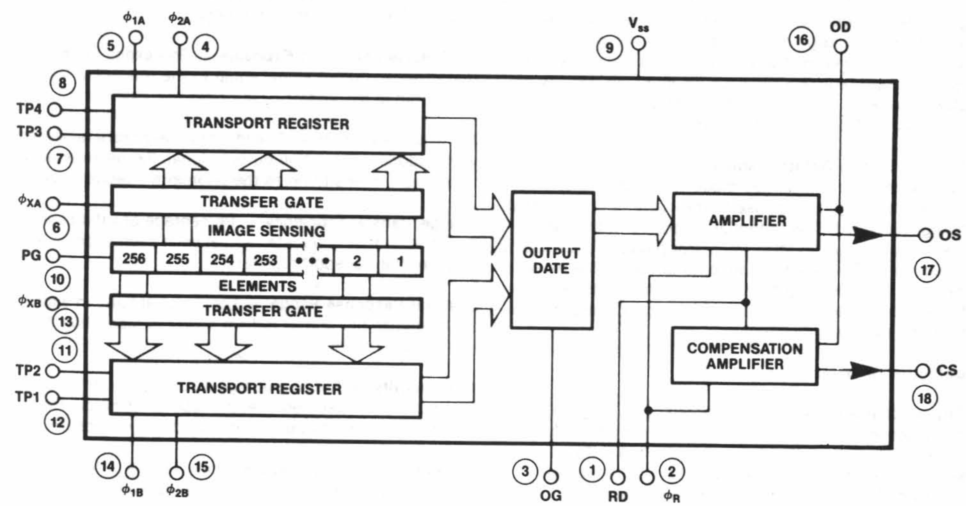


DIP (TOP VIEW)

Pin Names:

PG	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Clock
ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}	Transport Clocks
OG	Output Gate
OS	Output Source
OD	Output Drain
CS	Compensation Source
ϕ_R	Reset Clock
RD	Reset Drain
TP	Test Point
V_{ss}	Substrate (ground)

Block Diagram



CCD111

Functional Description
The CCD111 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 256 image sensor elements separated by a diffused channel stop and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the left and right transport registers. The transfer gates also control the integration time for the sensing elements.

Two 130-Bit Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output OS. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Definition of Terms

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Gated Charge Detector/Amplifier — The output circuit of the CCD111 that receives the charge packets from the transport registers and provides a signal voltage proportional to the size of each charge packet received. Before each new charge packet is sensed, a reset clock returns the charge detector voltage to a fixed level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. (This does not take into account dark signal components.) Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements. (See accompanying photos for details of definition.)

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation ouput voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — A picture element (photosite).

Peripheral Response — The output signal caused by light-generated charge that is collected by the transport registers (instead of the photosites). The device is covered, except over the photosites, by a gapped metal layer, which functions both as an array of interconnections and as a reflective light shield. The major component of Peripheral Response for visible light ($\lambda \leq 700$nm) is generated in the transport registers by light transmitted through these gaps in the metal above the registers. For near-infrared light ($\lambda \geq 700$nm), especially on CCD111A devices, a portion of the charge generated by light absorbed under the photosites and one transport register is collected in the opposite transport register.

Major Differences Between the CCD111A and CCD111B
Both the CCD111A and the CCD111B have the same responsivity to visible light (400-700nm). The principal differences are as follows:

The CCD111A is intended for use in applications where very low dark signal and high responsivity to very near-infrared (700-900nm) light are needed, and where peripheral response is not critical.

The CCD111B is selected for use in applications where standard responsivity to very near-infrared (700-900nm) light and standard dark signal are acceptable and where peripheral response needs to be minimized.

It is not recommended that either part be used with illumination containing wavelengths greater than 900nm (near-infrared). If use of such a light source (unfiltered tungsten, for example) is unavoidable, the CCD111B will generally provide the user with more satisfactory results. The table on performance characteristics provides more information.

Absolute Maximum Ratings

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15	−0.3V to 15V
Pins 1, 8, 11, 16	−0.3V to 18V
Pins 17, 18	output, no voltage applied
Pin 9	OV

Caution Note
This device has limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins OS and CS to V_{SS} or V_{OD} during operation of the device. Shorting these pins temporarily to V_{SS} or V_{OD} may destroy the output amplifiers.

DC Characteristics: T_c = 25°C (Note 1)

Symbol	Characteristic	Limits Min	Limits Typ	Limits Max	Unit	Condition
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	11.5	12.0	12.5	V	
V_{OG}	Output Gate Voltage		5.0		V	
V_{PG}	Photogate Voltage	9.5	10.0	12.5	V	
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CCD111

Clock Characteristics: T_c = 25°C (Note 1)

Symbol	Characteristic	Limits Min	Limits Typ	Limits Max	Unit	Condition
$V_{\phi 1AL}$, $V_{\phi 1BL}$, $V_{\phi 2AL}$, $V_{\phi 2BL}$	Transport Clocks LOW	0.0	0.5	0.8	V	Note 2
$V_{\phi 1AH}$, $V_{\phi 1BH}$, $V_{\phi 2AH}$, $V_{\phi 2BH}$	Transport Clocks HIGH	7.5	8.0	8.5	V	Note 5
$V_{\phi XAL}$, $V_{\phi XBL}$	Transfer Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V_{\phi XAH}$, $V_{\phi XBH}$	Transfer Clock HIGH	7.5	8.0	8.5	V	Note 5
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V_{\phi RH}$	Reset Clock HIGH	7.5	8.0	8.5	V	Notes 3, 5
$f_{\phi 1A}$, $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$	Maximum Transport Clock Frequency		5.0		MHz	Note 5
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Data Rate)		10.0		MHz	Note 6

AC Characteristics: T_c = 25°C, $f_{\phi R}$ = 1.0 MHz, t_{int} = 320 μs, $t_{transport}$ = 259 μs, Light Source = 2854°K + filters as specified. All operating voltages nominal specified values. (Note 1)

Symbol	Parameter	Range Min	Range Typ	Range Max	Unit	Condition
DR	Dynamic Range (relative to rms noise) (relative to peak-to-peak noise)	 1250:1 250:1	 2500:1 500:1			Note 7
NEE	RMS Noise Equivalent Exposure		2×10^{-4}		μJ/cm²	
SE	Saturation Exposure		0.5		μJ/cm²	
CTE	Charge Transfer Efficiency		99.995		%	Note 8
SR	Spectral Response Range Limits		0.45 – 1.05		μm	
P	Power Dissipation		100		mW	V_{OD} = 15V
Z	Output Impedance		1000		Ω	
N	RMS Noise Peak-to-Peak Noise		80 400		μV	

CCD111

Performance Characteristics: T_c = 25°C, $f_{\phi R}$ = 1.0 MHz, t_{int} = 320μs, $t_{transport}$ = 259μs,
Light Source = 2854°K + filters as specified.
All operating voltages nominal specified values. (Note 1)

Symbol	Characteristic	CCD111A Min	CCD111A Typ	CCD111A Max	CCD111B Min	CCD111B Typ	CCD111B Max	Unit	Condition
PRNU	Photoresponse Non-uniformity Peak-to-Peak								
	2854°K + 700 nm cutoff filter		35	70		25	70	mV	14, 15, 16
	2854°K + 900 nm cutoff filter		45	110		45	110	mV	14, 15, 16
	2854°K unfiltered		70			60		mV	14, 15, 16
	Single-pixel Positive Pulses		<10			<10		mV	15, 16
	Single-pixel Negative Pulses		20	60		20	60	mV	15, 16
RI	Register Imbalance ('Odd'/'Even')		<5			<5		mV	15, 16
DS	Dark Signal DC Component	0	<1	3	0	2	15	mV	2, 9, 10
	Low Frequency Component	0	<1	2	0	2	10	mV	2, 9, 11
SPDSNU	Single-pixel DS Non-uniformity	0	<1	2	0	1	2	mV	9, 11, 12
PR	Peripheral Response								
	2854°K + 700 nm cutoff filter		10	17		<2	5	% of V_{OUT}	14
	2854°K + 900 nm cutoff filter		12	20		3	7	% of V_{OUT}	14
	2854°K unfiltered		25			4		% of V_{OUT}	14
R	Responsivity								
	2854°K + 700 nm cutoff filter	0.7	1.3	2.1	0.5	1.1	2.0	V/μJ/cm²	13, 14
	2854°K + 900 nm cutoff filter	1.3	2.4	3.9	0.8	1.6	2.4	V/μJ/cm²	13, 14
	2854°K unfiltered		2.0			0.9		V/μJ/cm²	13, 14
V_{SAT}	Saturation Output Voltage	500	900		500	900		mV	17

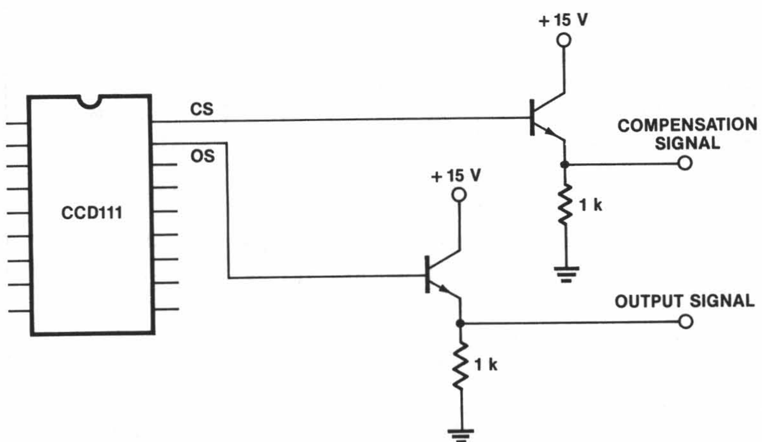
Notes

1. T_C is defined as the package temperature, measured on the back surface of the ceramic body.
2. Negative transients on any clock pin going below 0.0V may cause charge injection that results in an increase in the apparent Dark Signal.
3. $V_{\phi RH}$ should track V_{RD}.
4. The data output frequency $f_{\phi R}$ is twice that of each transport clock ($f_{\phi 1A}$, $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$).
5. $C_{\phi XA} \simeq C_{\phi XB} \simeq 20pF$, $C_{\phi 1A} \simeq C_{\phi 2A} \simeq C_{\phi 1B} \simeq C_{\phi 2B} \simeq 32pF$, $C_{\phi R} \simeq 5pF$.
6. Minimum reset clock frequency is limited by the increase in Dark Signal.
7. Dynamic Range is defined as "V_{SAT}/rms (temporal) Noise" or "V_{SAT}/Peak-to-Peak (temporal) Noise."
8. CTE is measured for a one-stage transfer.
9. See photographs for Dark Signal definitions.
10. DC and low-frequency Dark Signal components approximately double for every 5°C increase in T_C. The shift register component is also inversely proportional to $f_{\phi R}$.
11. Single-pixel Dark Signal non-uniformity (SPDSNU) approximately doubles for every 8°C increase in T_C. They are also directly proportional to the integration time t_{int}.
12. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU.
13. RESPONSIVITY is defined as the "volts of video output" per "Incident Radiant Energy measured over the 350 nm–1200 nm band." The device will not respond to infrared wavelengths longer than ≈ 1200 nm. However, 2/3 of the radiant energy from a 2854°K source is at $\lambda > 1200$ nm. For the unfiltered 2854°K source, the responsivity values for light measured over $0 < \lambda < \infty$ will be ~0.3X of the responsivity values for light measured over 350 nm $< \lambda <$ 1200 nm.

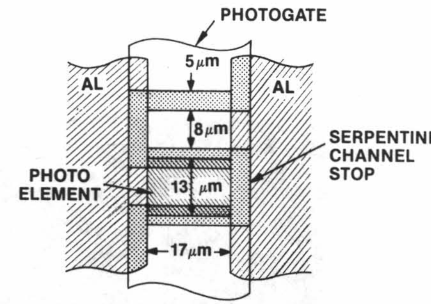
Notes (cont'd)

14. OPTICAL FILTERS: a "700 nm cutoff" filter is realized by using one "Wide Band Hot Mirror" (Optical Coating Labs, Inc., Santa Rosa, California) and one 2.0 mm thick "BG-38" blue glass (Schott Optical Glass, Duryea, Pennsylvania) filter in series. The "900 nm cutoff" filter is available on special order; consult Fairchild CCD Applications Engineering for details. Transmittance curves for the two cutoff filters and Spectral Energy Distribution curves for these filters with a 2854°K light source are given in the "Typical Performance Curves" section of this data sheet. It should be noted that the "2854°K + 700 nm cutoff" source is a good approximation to a Daylight Fluorescent bulb.
15. All PRNU measurements taken at a 350mV output level using a F/5.0 lens; all PRNU measurements exclude the outputs from the first and last photoelements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As f number increases, the resulting more highly collimated light causes package window aberrations to dominate and increase the PRNU. A lower f number (f ≤ 5) results in less collimated light, causing photosite blemishes to dominate PRNU.
16. See photographs for PRNU definitions.
17. See test load configuration.

Test Load Configuration

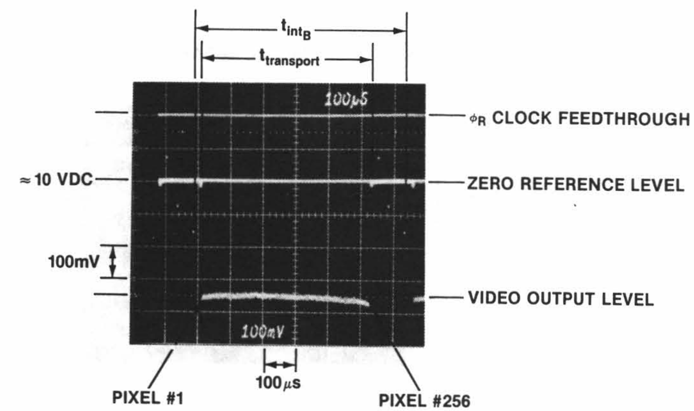


Photoelement Dimensions



ALL DIMENSIONS ARE TYPICAL VALUES.

Output with Uniform Illumination

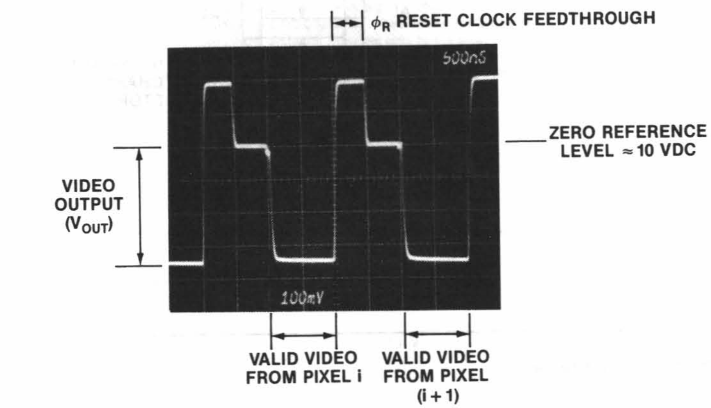


TEST CONDITIONS: $T_C = +25°C$, $t_{int} = 640\ \mu s$, $f_{\phi R} = 512$ kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

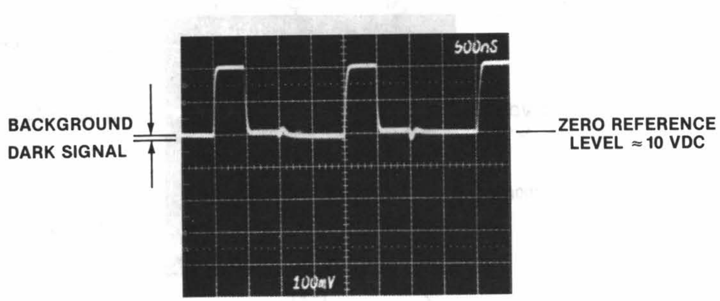
CCD111

Output of Two Pixels

DEVICE ILLUMINATED



DEVICE IN DARK

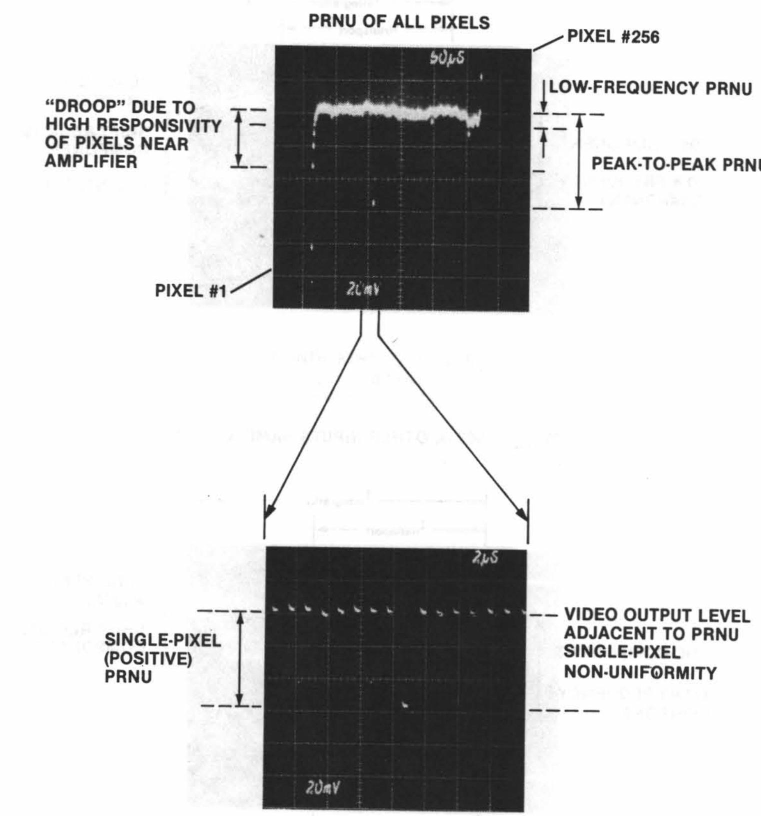


TEST CONDITIONS: T_C = +25°C, t_{int} = 640 μs, $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

CCD111

Photoresponse Non-uniformity

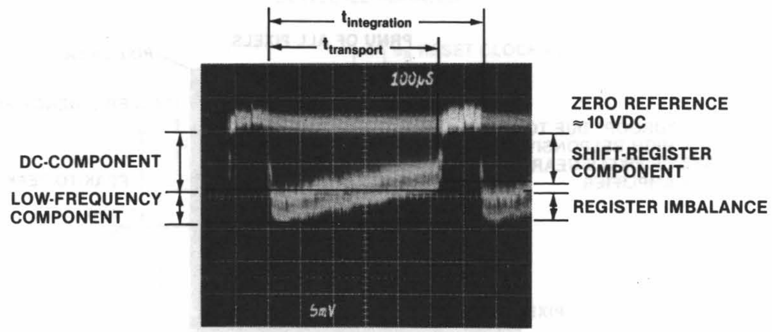
MEASURED AT V_{OUT} = 350 mV; ALL PRNU COMPONENTS EXCLUDE PIXELS #1 AND #256.



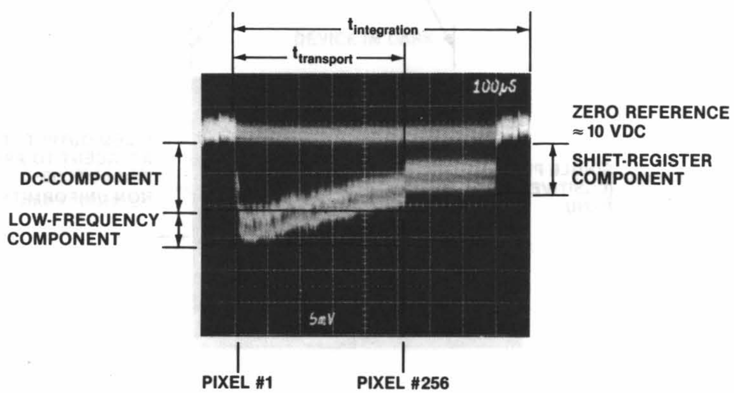
TEST CONDITIONS: T_C + 25°C, t_{int} = 320 μs, $f_{\phi R}$ = 1.0 MHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set.

DC + Low Frequency Dark Signal

AT t_{int} = 640μs:

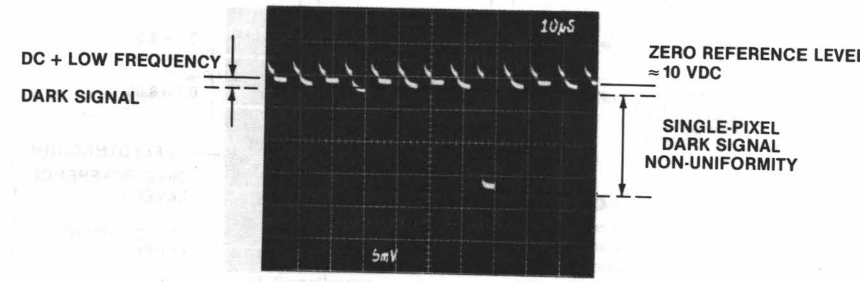


AT t_{int} = 900μs, OTHER INPUTS SAME AS ABOVE:



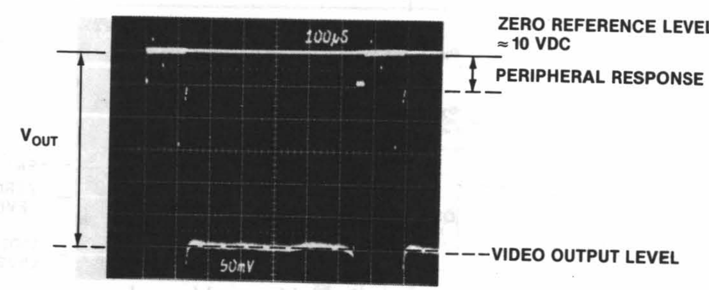
TEST CONDITIONS: T_C = +25°C, t_{int} = (see above), $f_{\phi R}$ = 512 kHz, "typ" voltage inputs. (Half standard test speeds for clearer photos.)

Single-pixel Dark Signal Non-uniformity



TEST CONDITIONS: T_C = +25°C, t_{int} = 2.560 ms, $f_{\phi R}$ = 128 kHz, "typ" voltage inputs. (One-eighth standard test speeds to emphasize Dark Signal.)

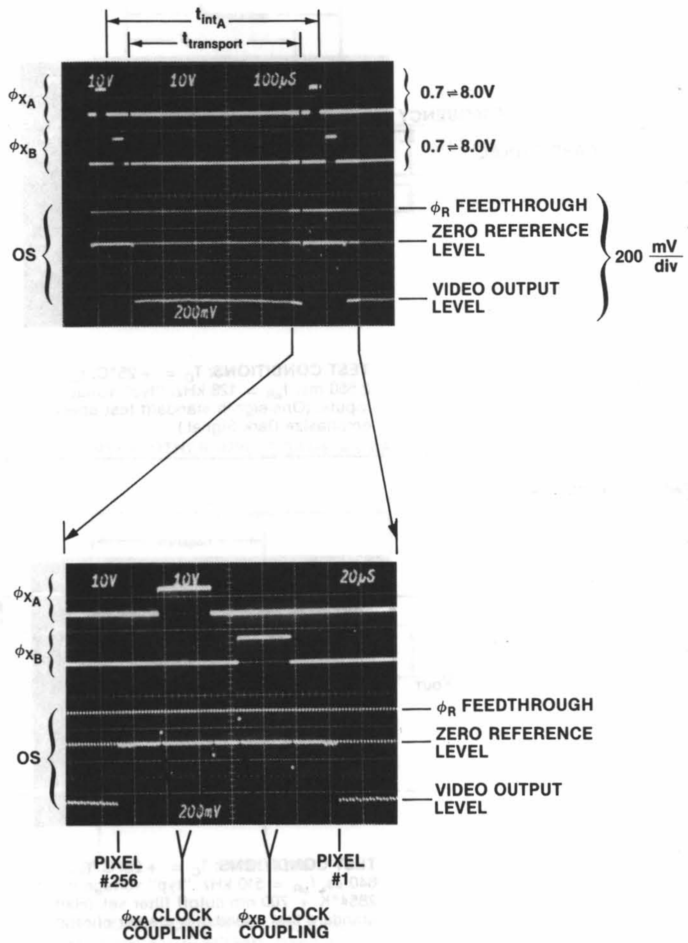
Peripheral Response



TEST CONDITIONS: T_C = +25°C, t_{int} = 640 μs, $f_{\phi R}$ = 510 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

CCD111

ϕ_X(Transfer Clock) Coupling into OS (Output)



TEST CONDITIONS: $T_C = +25°C$, $T_{int} = 640\ \mu s$, $f_{\phi R} = 512$ kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

CCD111

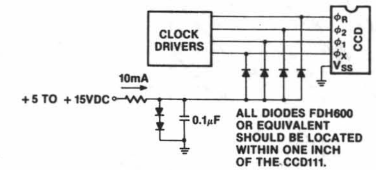
Device Care and Operation

Charge Injection: Every input pin has a gate protection structure that includes a diode from the input to the (grounded) substrate V_{SS}. The diode is reverse-biased during normal operation ($V_{in} > V_{SS}$). Negative (transient) input voltages ($V_{in} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chip.

If sufficient charge is injected, it will accumulate in the transport register(s) and/or the photosites near the injecting gate protection structure(s). Injected charge which accumulates in the photosites will typically result in an apparent bell-shaped increase in Dark Signal (≈ 20-200 pixels wide) near the injecting gate protection structure. Injected charge which accumulates in a transport register will result in an apparent uniform increase in that register's low frequency dark signal, creating a noticeable increase in the apparent Register Imbalance ("odd/even") of the Dark Signal.

The susceptibility to charge injection sufficient to increase the DC and Low Frequency Dark Signal varies significantly from device to device. It is not possible to select devices with "low" susceptibility. However, devices with low Dark Signal are typically more susceptible than devices with high Dark Signal.

Sufficient charge to appear as increased DC and Low Frequency Dark Signal may be injected by negative transient voltages <4 ns long. Since these transients cannot be detected by oscilloscopes with less than 250-500 MHz bandwidth, a system which appears to be free from negative transients on a 200 MHz scope may still be prone to charge injection. The recommended method to eliminate charge injection is the following diode clipper circuit:

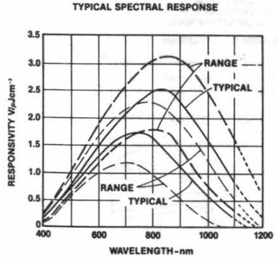


It is also important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The DC and Low Frequency Dark Signal approximately doubles for every 5°C temperature increase and Dark Signal Non-Uniformities approximately double for every 8°C increase. The devices may be cooled to achieve very long integration times and very low light level capability.

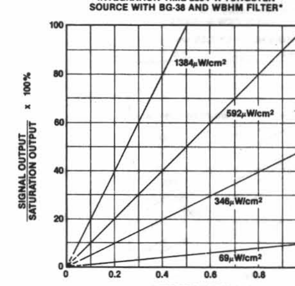
Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

Typical Performance Curves

TYPICAL SPECTRAL RESPONSE



OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTER*



*See note 14, page 6.

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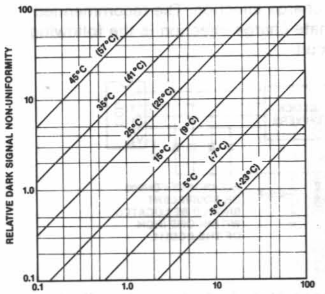
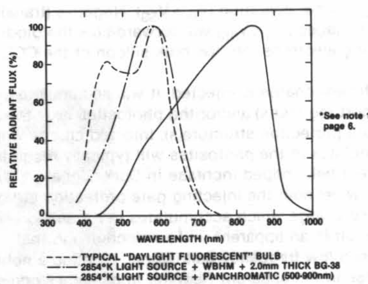
Typical Performance Curves (cont'd)

DARK SIGNAL NON-UNIFORMITY VERSUS INTEGRATION TIME

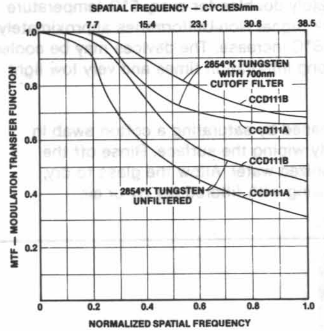


NOTE:
DC and low-frequency dark signal temperature in bold and SPDSNU in (parentheses).

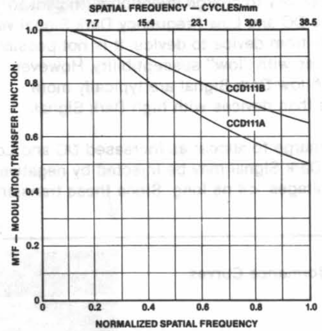
RELATIVE RADIANT FLUX VERSUS WAVELENGTH*



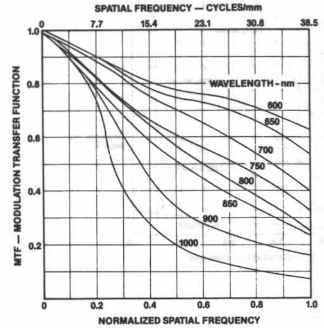
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



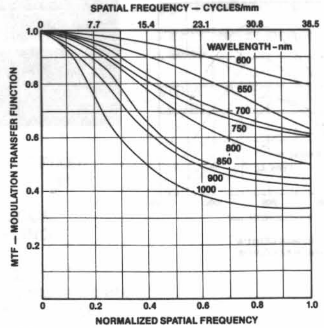
MODULATION TRANSFER FUNCTIONS FOR A 500nm-900nm BANDPASS ILLUMINATION SOURCES



CCD111A MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES

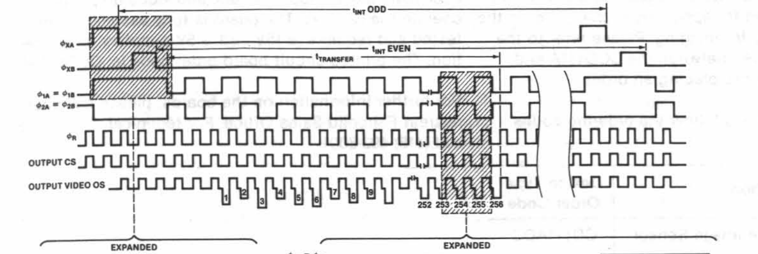


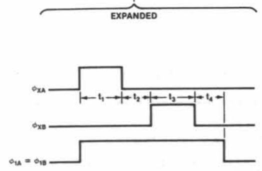
CCD111B MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



CCD111

Timing Diagram Drive Signals





Timing requirements for transfer Gate Pulses ϕ_{XA}, ϕ_{XB}
No requirement for t_2 · ϕ_{XA} may be tied to ϕ_{XB}

$t_1 = t_3 > 0.8\mu s$
$t_4 > 0.1\mu s$

$20ns < (t_r = t_f) < 80ns$

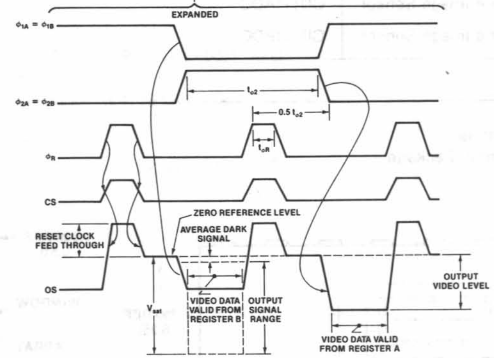
Timing requirements for Reset Pulse ϕ_R

$t_r = t_f < 20ns$
$0.2(t_{\phi 2}) < t_{\phi R} < 0.3(t_{\phi 2})$

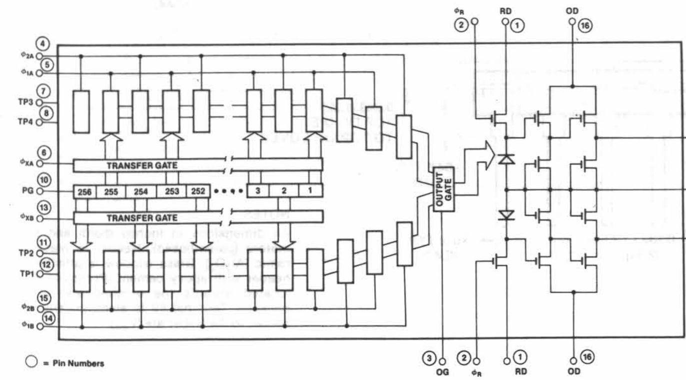
Timing requirements for ϕ_{1A}, ϕ_{1B}

$20ns < (t_r = t_f) < 100ns$

ϕ_1 and ϕ_2 clocks may not both be < 3.5V simultaneously.



Circuit Diagram



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Order Information
It is important to note that two different selections of the CCD111 are being offered for applications that differ in the wavelength of light used for imaging. Please refer to the section "Major Differences Between the CCD111A and CCD111B" on page 3 before placing an order.

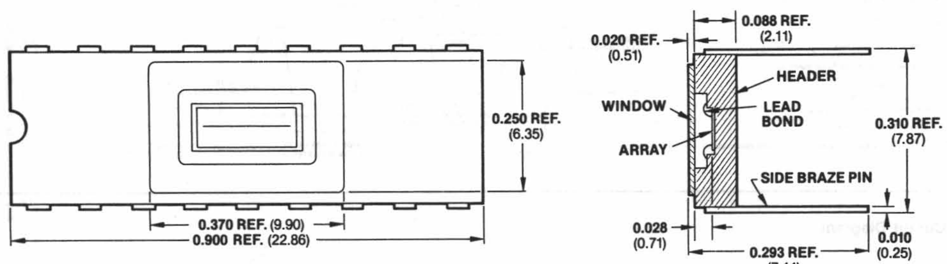
To order the CCD111, please follow the ordering codes listed in the table below:

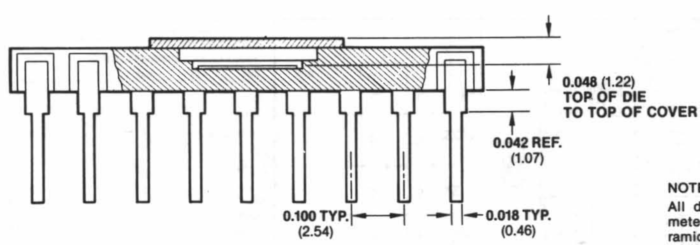
Description	Device Type Order Code
CCD111A 256 x 1 Line Image Sensor	CD111ADC
CCD111B 256 x 1 Line Image Sensor	CD111BDC

A printed circuit board is available which includes all the necessary clocks, logic drivers, and video amplifiers to operate the CCD111. The board is fully assembled and tested and requires ±15V and +5V supplies for operation. The printed circuit board order code is: CCD111DB.

For further information on the boards, please call your nearest Fairchild Sales Office. For technical assistance, call (415) 493-8001.

CCD111DC Package Outline
18-Pin Dual In-Line Ceramic Package





NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement. Photosite #1 is located towards the notched end of the package. Terminal #9 is electronically connected to the Substrate (V_{SS}).

CCD121H
1728-ELEMENT LINEAR IMAGE SENSOR
CHARGE COUPLED DEVICE

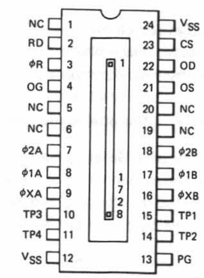
GENERAL DESCRIPTION – The CCD121H is a monolithic self-scanned 1728-Element Image Sensor designed for page scanning applications. The device provides a 200-line per inch resolution across an 8-1/2 inch page. Other intended applications are: facsimile readers, optical character recognition, as well as imaging applications that require high resolution, high sensitivity and high speed.

In addition to a row of 1728 sensing elements, the CCD121H chip includes: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 1728 imaging elements.

The cell size is 13μ (0.51 mils) by 17μ (0.67 mils) on 13μ (0.51 mils) centers. The device is manufactured using Fairchild charge coupled device buried-channel technology.

- DYNAMIC RANGE TYPICAL: 500:1 (PEAK-TO-PEAK), 2500:1 (rms)
- 1728 ELEMENTS ON A SINGLE CHIP
- ON-CHIP PREAMPLIFIER AND COMPENSATION AMPLIFIER
- LOW POWER REQUIREMENTS
- ALL OPERATING VOLTAGES UNDER 15 V
- PACKAGED IN A 24-PIN DUAL IN-LINE HERMETIC PACKAGE
- LOW NOISE EQUIVALENT EXPOSURE
- WIDE RANGE OF VIDEO DATA RATE
- DIMENSIONALLY PRECISE PHOTOSITE SPACING

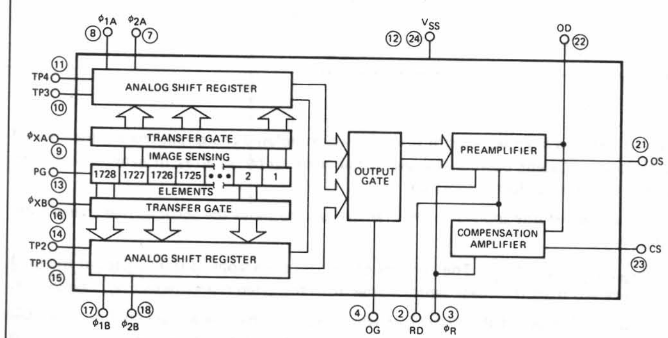
CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

PG	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Gate Clocks
ϕ_{1A}, ϕ_{2A} ϕ_{1B}, ϕ_{2B}	Analog Shift Register Transport Clocks
OG	Output Gate
OS	Output Transistor Source
OD	Output Transistor Drain
CS	Compensation Transistor Source
ϕ_R	Reset Transistor Gate Clock
RD	Reset Transistor Drain
TP	Test Point
V_{SS}	Substrate (Ground)
NC	No Connection

BLOCK DIAGRAM



CCD121H

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	-25°C to 100°C
Operating Temperature	-25°C to 55°C
Pins 3, 4, 7, 8, 9, 10, 13, 15, 16, 17, 18	-0.3 V to 12 V
Pins 2, 11, 14, 21, 22, 23	-0.3 V to 18 V

Caution Note: The device has limited built-in gate protection. It is recommended to control and minimize static charge buildup. Care should be taken to avoid shorting leads OS and CS to ground during operation of the device.

FUNCTIONAL DESCRIPTION —The CCD121H consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 1728 Image Sensor Elements separated by diffused channel stops and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon by hole-electron pair production. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. The output signal will vary in this analog manner from a thermally generated noise background at zero illumination to a maximum at saturation.

Two Transfer Gates — Gate structures adjacent to the row of Image Sensor Elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers. Alternating charge packages are transferred to the left and right (A and B) analog transport shift registers. The HIGH states of the transfer-gates must be contained by the HIGH state of the transport shift register clocks. The next light integration period is started when transfer gates go LOW.

Two 866-Bit Analog Shift Registers — One on each side of the row of Image Sensor Elements and separated from it by a Transfer Gate. The two registers are used to move the image generated charge packets serially from the sensor elements to the charge detector/preamplifier. The phase relationship of the last elements of the two shift registers provide for alternate delivery of charge packets to re-establish the serial sequence of the photosites.

A Gated Charge Detector/Preamplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal output at OS. The reset transistor is driven by a reset clock (ϕ_R) so as to recharge the charge-detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

DEFINITION OF TERMS

Charge Coupled Device — A charge coupled device is a semiconductor device in which isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking by an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Gate Clock ϕ_{XA}, ϕ_{XB} — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD shift registers.

Analog Shift Register Transport Clocks, ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase clock applied to the gates of the CCD shift registers to move the charge packets received from the image sensor elements to the gated charge-detecting preamplifier.

Gate Charge Detector Preamplifier — The output circuit of the CCD121H which receives the charge packets from the CCD shift registers and provides a signal voltage proportional to the size of each charge packet. Before each new charge packet is sensed, a reset clock returns the output voltage to a base level.

Reset Clock ϕ_R — The voltage waveform required to drive the gated charge detector preamplifier.

Dynamic Range — The saturation exposure divided by the peak-to-peak noise equivalent exposure.

This does not take into account dark signal non-uniformities or average dark signal. Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of 4 to 6 is generally appropriate. (Peak-to-peak noise is approximately equal to 4 to 6 times rms noise.)

DEFINITION OF TERMS (Cont'd)

Peak-to-Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Saturation exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. This is commonly expressed as a percentage of the saturation output voltage.

Average Dark Signal — The output signal level in the dark averaged over all elements and measured relative to the base line output voltage established by the reset clock. This is a linear function of the integration time. It is also strongly dependent on temperature. This is commonly expressed as a percentage of the saturation output voltage.

Dark Signal Non-uniformity — Maximum deviation of the output voltage of any element from the background level in the dark. This is commonly expressed as a percentage of the saturation voltage.

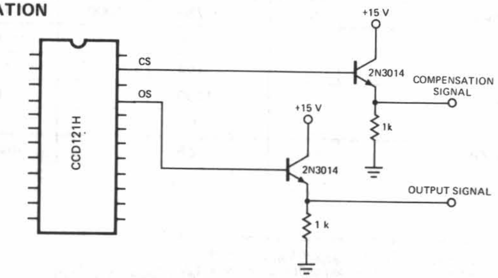
Saturation Output Voltage — The maximum signal output voltage.

Integration Time — The time interval between the falling edges of any transfer pulse ϕ_{XA} and ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Output Signal Range — The output signal range is defined as OSR = $V_{sat} - (t_{INT} + t_{Transport})$ X Rate of Average Signal Offset where: t_{INT} = Integration Time; $t_{Transport}$ = time necessary to transfer the charge packets from the analog shift registers and is equal to $\frac{1728}{f\phi_R}$. Integration time (t_{INT}) does not necessarily equal transfer time ($t_{Transport}$). If long integration times are required, $t_{Transport}$ should be minimized (increase $f\phi_R$) to maximize OSR.

Average Signal Offset — Average signal offset is a dc offset of the output voltage (due to the average leakage current in the CCD registers) which increases linearly with the transfer time.

TEST LOAD CONFIGURATION



DC CHARACTERISTICS: T_A = 25°C

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	11.5	12.0	12.5	V	Note 1
V_{OG}	Output Gate Voltage	4.5	5.0	5.5	V	
V_{PG}	Photogate Voltage	10.0	10.3	10.5	V	
TP1, TP3	Test Points		0.0		V	Connect to V_{SS}
TP2, TP4	Test Points	14.5	15.0	15.5	V	

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CLOCK CHARACTERISTICS: $T_A = 25°C$

SYMBOL	CHARACTERISTIC	RANGE MIN	TYP	MAX	UNITS	CONDITIONS
$V_{\phi 1AL}, V_{\phi 1BL}$ $V_{\phi 2AL}, V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Notes 2, 3
$V_{\phi 1AH}, V_{\phi 1BH}$ $V_{\phi 2AH}, V_{\phi 2BH}$	Analog Shift Register Transport Clocks HIGH	7.5	8.0	8.5	V	Note 3
$V_{\phi XAL}$	Transfer Gate Clock LOW	0.0	0.5	0.8	V	Notes 2, 3
$V_{\phi XAH}$	Transfer Gate Clock HIGH	7.5	8.0	8.5	V	Note 3
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 2, 3
$V_{\phi RH}$	Reset Clock HIGH	7.5	8.0	8.5	V	Note 3
$f_{\phi 1A}, f_{\phi 1B}$ $f_{\phi 2A}, f_{\phi 2B}$	Maximum Analog Shift Register Transport Clock Frequency		5.0		MHz	Notes 4, 5
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Bit Rate)		10.0		MHz	Notes 4, 5

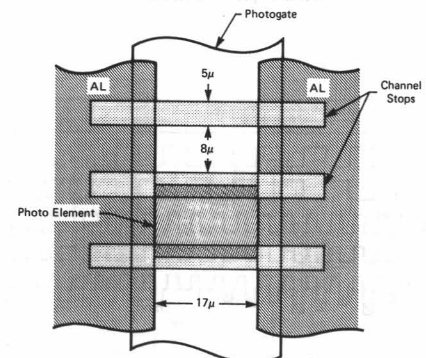
AC CHARACTERISTICS: $T_A = 25°C$, $f_{\phi 1} = f_{\phi 2} = 0.5$ MHz, $f_{\phi R} = 1$ MHz, $t_{INT} \cong 1.78$ ms, $t_{TRANSPORT} = 1.73$ ms, See Note 14.

SYMBOL	CHARACTERISTIC	RANGE MIN	TYP	MAX	UNITS	CONDITIONS
DR	Dynamic Range	250	500			Notes 6, 7
NEE	Peak-to-Peak Noise Equivalent Exposure		1×10^{-3}		$\mu j/cm^2$	Note 7
SE	Saturation Exposure		1.0		$\mu j/cm^2$	Note 7
SR	Spectral Response Range Limits		0.45–1.05		μm	
R	Responsivity		0.5		V per $\mu j/cm^2$	Notes 9, 10, 11
PRNU	Photoresponse Non-uniformity		±25	±50	mV	Note 8
ADS	Average Dark Signal		5.0	25	mV	Note 12
DSNU	Dark Signal Non-uniformity		20	50	mV	Note 13
V_{sat}	Saturation Output Voltage	500	750	1000	mV	Notes 9, 10
V_O	Output DC Level		7.5		V	
P	Power Dissipation		165		mW	$V_{OD} = 15$ V
Z	Output Impedance		1000		Ω	
N	Peak-to-Peak Noise		1.0		mV	
RSO	Rate of Average Signal Offset		2.5		mV/ms	

NOTES:
1. $V_{\phi RH}$ should track V_{RD}.
2. Negative transients on the clocks below 0.0 V may cause an increase in apparent dark signal.
3. $C_{\phi XA} = C_{\phi XB} = C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} \cong 400$ pF, $C_{\phi RA} = C_{\phi RB} \cong 10$ pF.
4. The resulting data output frequency is twice that of each analog shift register clock, $f_{\phi 1A}, f_{\phi 2A}, f_{\phi 1B}, f_{\phi 2B}$.
5. Minimum clock frequency is limited by increase in dark current which reduces output signal range OSR. See curves.
6. The dynamic range is measured by taking the ratio of the saturation output voltage to the peak-to-peak noise of the device in the dark. Because of the high degree of linearity of the device the dynamic range measurement is also approximately equal to the ratio of the saturation exposure to the peak-to-peak noise equivalent exposure.
7. 1 $\mu j/cm^2$ = 0.02 fcs at 2854°K, 1 fcs = 50 $\mu j/cm^2$ at 2854°K.
8. Measurement is done at ≈ 350 mV output level. Measurement excludes first and last elements but includes both registers' outputs.
9. See test load configurations.
10. See definition of terms.
11. For 2854°K light source.
12. See curve.
13. DSNU has similar integration time and temperature dependence as ADS.
14. It is recommended to use an infrared blocking filter to obtain minimum PRNU and crosstalk.

CCD121H

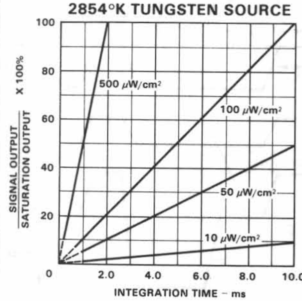
PHOTOELEMENT DIMENSIONS



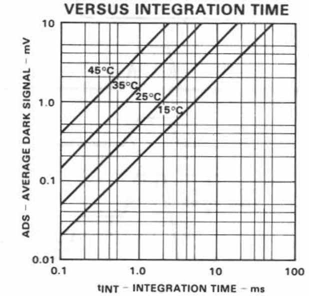
All dimensions are typical values

TYPICAL PERFORMANCE CURVES

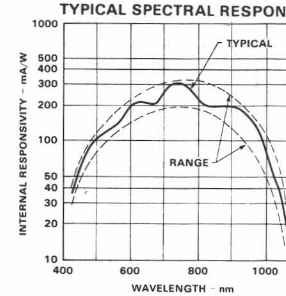
OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE



AVERAGE DARK SIGNAL VERSUS INTEGRATION TIME

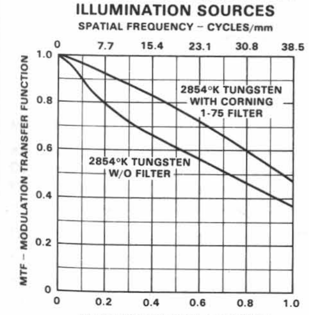


TYPICAL SPECTRAL RESPONSE



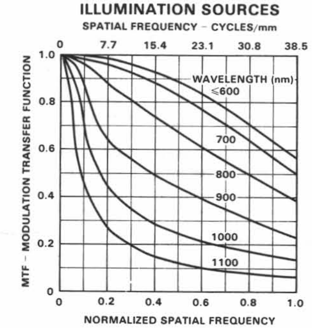
Note 1. Internal responsivity is related to the responsivity at the output through integration time and preamp charge-to-voltage conversion gain.
Note 2. Internal responsivity pertains to photoelement signal only; it excludes the shift in black reference level produced by long wavelength radiation.

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



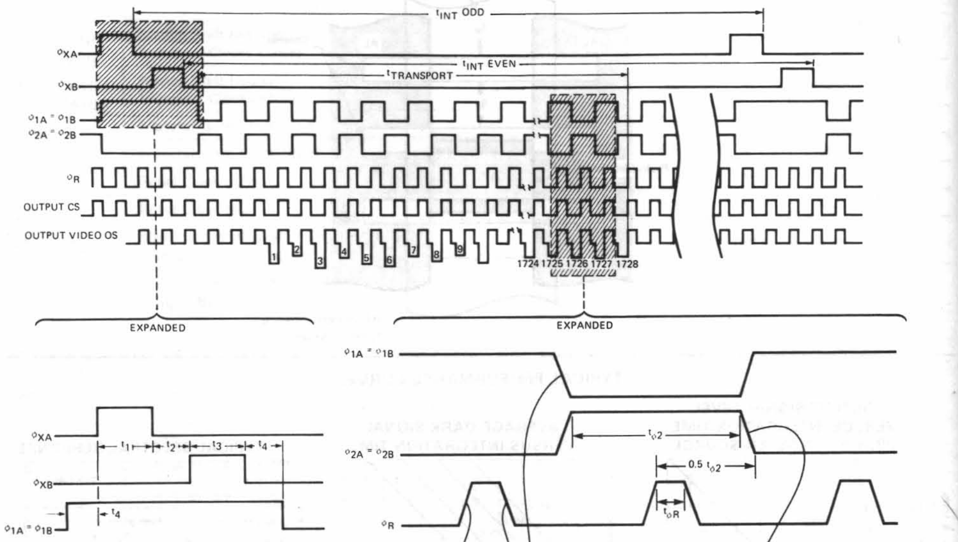
The Corning 1-75 filter has the following typical transmittance spectral characteristic: >85% at <600 nm, 60% at 700 nm, 30% at 800 nm, 5% at 900 nm and <2% at >1000 nm.

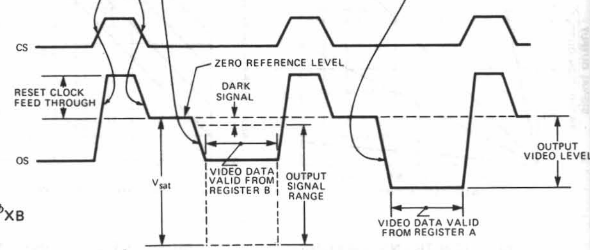
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



CCD121H

TIMING DIAGRAM DRIVE SIGNALS





Timing requirements for Transfer Gate Pulses ϕ_{XA}, ϕ_{XB}

$t_1 = t_3 > 0.8\ \mu s$

$t_2 = t_4 > 0.1\ \mu s$

Timing requirements for Reset Pulse ϕ_{RA}

$t_r = t_f < 0.3\ (t\phi_R)$

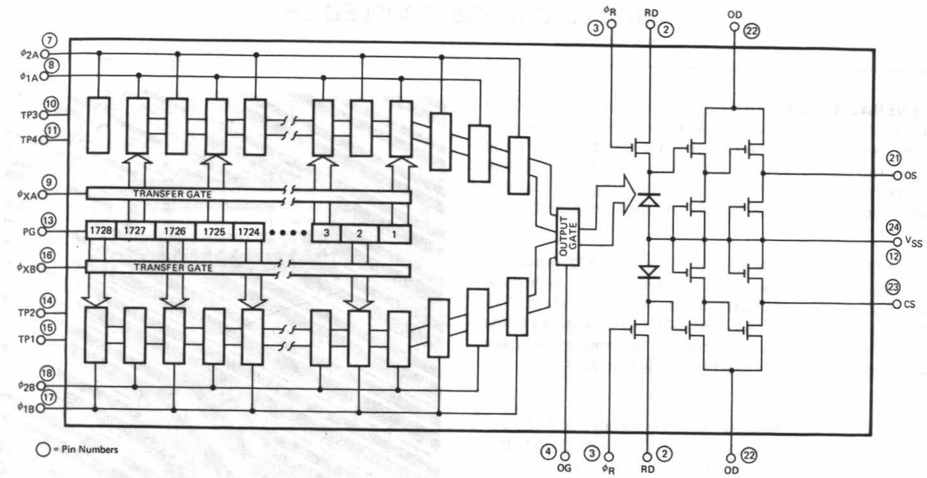
$0.25\ (t\phi_2) < t\phi_R < 0.5\ (t\phi_2)$

Timing requirements for $\phi_{1A} = \phi_{1B}$

$0.1\ (t\phi_2) < (t_r = t_f) < 0.4\ (t\phi_2)$

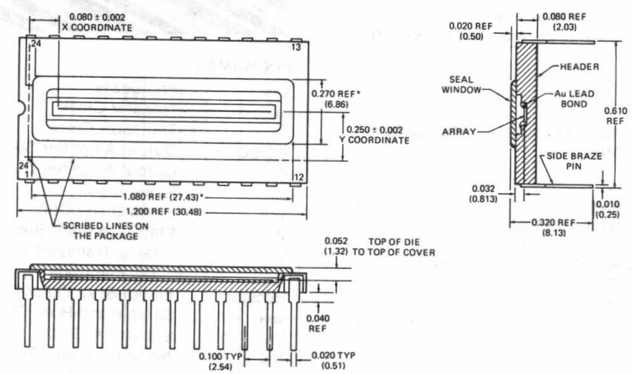
CCD121H

CIRCUIT DIAGRAM



PACKAGE OUTLINE

24-Pin Dual In-line Hermetic Package



NOTES:

All dimensions in inches (bold) and millimeters (parenthesis). Header is black ceramic (Al_2O_3). Transparent portion of package is glass. The CCD121H hermetic package carries the number "24" close to pin 1 of the device. This number should not be confused with pin 24 of the device is connected to V_{SS} (substrate).

ORDER INFORMATION – Order CCD121HC where "H" stands for hermetic package and "C" is commercial temperature range. The CCD121HC is the replacement for the CCD121DC. The two devices are pin-for-pin compatible. The output on-chip amplifier of the CCD121H is an improved design (over the CCD121) providing a higher saturation output voltage of typically 750 mV.

Also available is a printed circuit board that includes all the necessary clocks, logic, drivers and video amplifiers to operate the CCD121H. The printed circuit board is fully assembled and tested and requires three power supplies for operation (+5 V, +15 V and –15 V). The printed circuit board order code is: CCD121HB.

FAIRCHILD
A Schlumberger Company

CCD

CCD122/142

1728/2048-ELEMENT LINEAR IMAGE SENSOR
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION—The CCD122 and CCD142 are monolithic 1728 and 2048-element line image sensors, respectively. The devices are designed for page scanning applications including facsimile, optical character recognition and other imaging applications which require high resolution and high sensitivity.

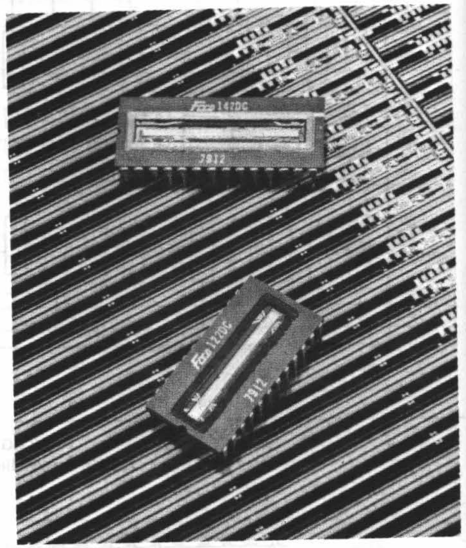
The 1728 sensing elements of the CCD122 provide a 200-line per inch resolution across an 8-1/2 inch page adopted as an international facsimile standard. The 2048 sensing elements of the CCD142 provide an 8-line per millimeter resolution across a 256 millimeter page adopted as the Japanese facsimile standard.

The CCD122 and the CCD142 have overall improved performance compared with the CCD121H including higher sensitivity, an enhanced blue response and a lower dark signal. The devices also incorporate on-chip clock driver circuitry.

The photoelement size is 13 μ (0.51 mils) by 13 μ (0.51 mils) on 13 μ (0.51 mils) centers. The devices are manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

- ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)
- LOW DARK SIGNAL
- HIGH RESPONSIVITY
- ON-CHIP CLOCK DRIVERS
- DYNAMIC RANGE TYPICAL: 2500:1
- OVER 1V PEAK-TO-PEAK OUTPUT
- DARK AND WHITE REFERENCES CONTAINED IN A SAMPLED-AND-HELD OUTPUT
- SINGLE POWER SUPPLY

533-00

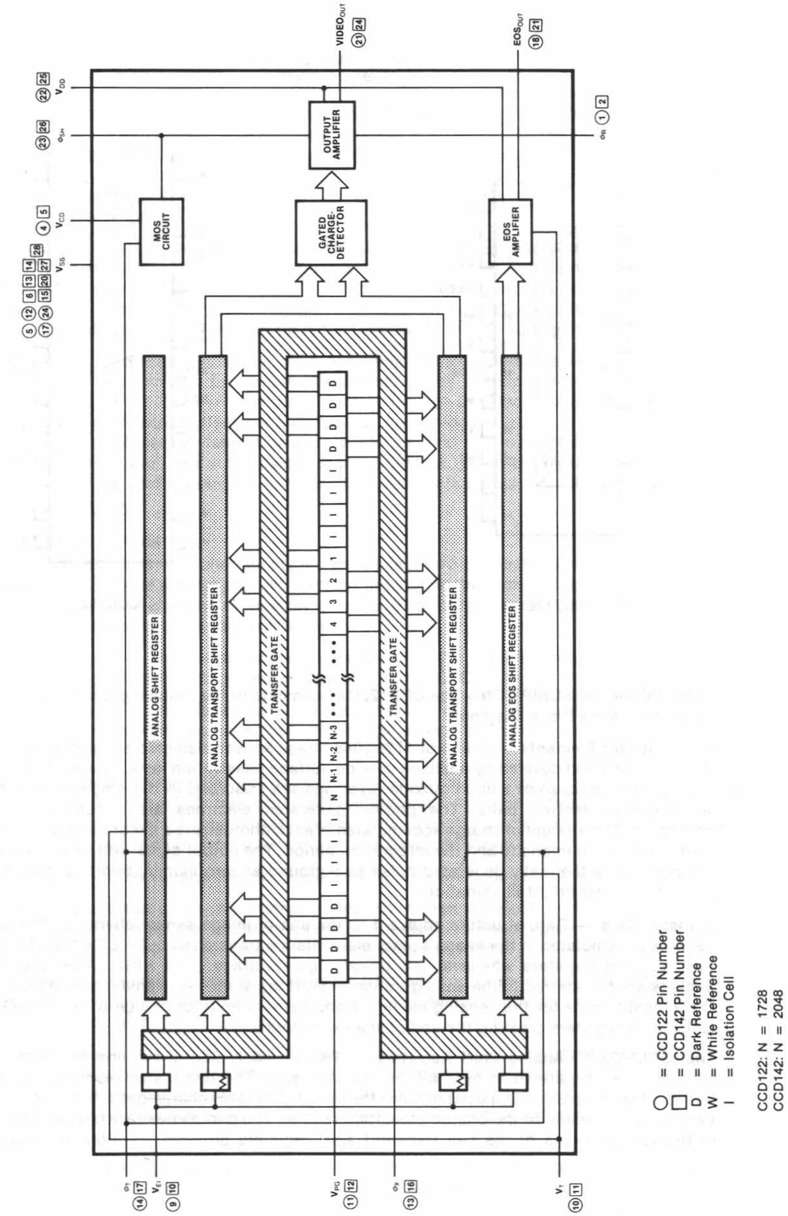


PIN NAMES

V_{PG}	Photogate
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
$VIDEO_{OUT}$	Output Amplifier Source
V_{DD}	Output Amplifier Drain
ϕ_R	Reset Clock
V_{CD}	Clock Driver Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
EOS_{OUT}	End-of-Scan Output
ϕ_{SH}	Sample-and-Hold Clock
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

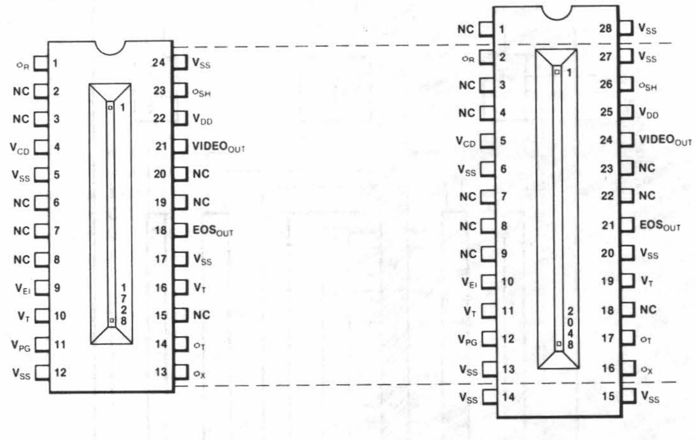
CCD122/142 VS. CCD121H COMPARISON

PARAMETER	CCD122/142	CCD121H
Spectral Response — Blue	4:1 Improvement	—
Overall	2:1 Improvement	—
Dark Signal	2:1 Improvement	—
Responsivity	2:1 Improvement	—
On-Chip Clock Drivers	Yes	No
Dark and White References	Yes	No
Single Power Supply	Yes	No



BLOCK DIAGRAM

CONNECTION DIAGRAM
DIP (TOP VIEW)



CCD122 CCD142

FUNCTIONAL DESCRIPTION—The CCD122/142 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A line of 1728/2048 image sensor elements separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate — Gate structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements and permits entry of charge to the End-Of-Scan (EOS) shift registers creating the end-of-scan waveform.

Four 879/1039-Bit Analog Shift Registers — Two on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside resisters, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the charge-detector/amplifier. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of charge-packets to establish the original serial sequence of the line of video in the output circuit. The outer two registers serve to deliver the end-of-scan waveform and reduce peripheral electron noise in the inner shift registers.

Gated Charge-Detector/Amplifier — Charge-packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sampled-and-held waveform. A reset transistor is driven by the Reset Clock (ϕ_R) and recharges the charge-detector diode capacitance before the arrival of each new signal charge-packet from the transport registers.

Clock Driver Circuitry — Allows the CCD122/142 to be operated using only three external clocks, (1) a Reset Clock signal which controls the integrated output signal amplifier, (2) a square wave Transport Clock which operates at half the reset clock frequency and controls the readout rate of video data from the sensor, and (3) a Transfer Clock pulse which controls exposure time of the sensor. The external clocks should be able to supply TTL level power.

Dark and White Reference Circuitry — Four additional sensing elements at both ends of the 1728/2048 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video ouptut representing the illuminated 1728/2048 sensor elements (labelled "D" in the block diagram). Also included at one end of the 1728/2048 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labelled "W" in the block diagram). These reference levels are useful as inputs to external DC restoration and/or automatic gain control circuitry.

DEFINITION OF TERMS:

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T — The clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifier.

Gated Charge-Detector/Amplifier — The output circuit of the CCD122/142 which receives the charge-packets from the CCD transport shift registers and provides a signal voltage proportional to the size of each charge-packet received. Before each new charge-packet is sensed, a reset clock returns the charge-detector voltage to a fixed base level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge-detector.

Sample-and-Hold Clock ϕ_{SH} — An internally supplied voltage waveform applied to the sample-and-hold gate in the amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting ϕ_{SH} to V_{DD}.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization providing a reference voltage equivalent to device operation in the dark. Permits use of external dc restoration circuitry.

White Reference — Video output level generated by on-chip circuitry providing a reference voltage permitting external automatic gain control circuitry to be used. The reference voltage is produced by charge-injection under the control of the electrical input bias voltage (V_{EI}). The amplitude of the reference is typically 70% of the saturation output voltage.

Isolation Cell — A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark and white reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the peak-to-peak noise equivalent exposure. (This does not take into account any dark signal components.) Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

Peak-to-Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal — The output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of defintion.)

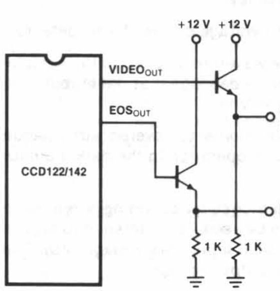
Total Photoresponse Non-Uniformity — The difference of the response levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum usable signal output voltage, measured from the zero reference level. (See timing diagram.) Any photoelement whose video output < saturation output voltage has an in-spec charge transfer efficiency (CTE). CTE will be below the specification if the video output ≥ saturation output voltage.

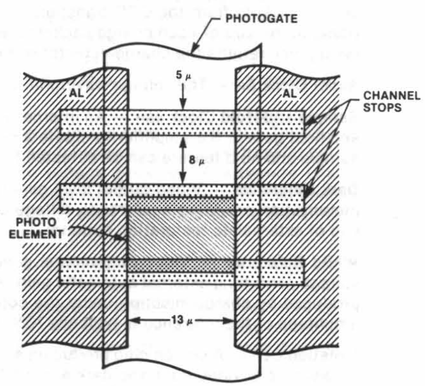
Integration Time — The time interval between the falling edges of any two successive transfer pulses ϕX as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite).

TEST LOAD CONFIGURATION



PHOTOELEMENT DIMENSIONS



All dimensions are typical values

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature		−25°C to +125°C
Operating Temperature (See curves)		−25°C to +70°C
CCD122:	Pins 1, 4, 9, 10, 11, 13, 14, 16, 22, 23	−0.3 V to 15 V
	Pins 5, 12, 17, 24	0 V
	Pins 2, 3, 6, 7, 8, 15, 18, 19, 20, 21	NC
CCD142:	Pins 2, 5, 10, 11, 12, 16, 17, 19, 25, 26	−0.3 V to 15 V
	Pins 6, 13, 14, 15, 20, 27, 28	0 V
	Pins 1, 3, 4, 7, 8, 9, 18, 21, 22, 23, 24	NC

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ and EOS_{OUT} to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{CD}	Clock Driver Drain Supply Voltage	12.0	13.0	14.0	V	
I_{CD}	Clock Driver Drain Supply Current		6.9	12.5	mA	
V_{DD}	Output Amplifier Drain Supply Voltage	12.0	13.0	14.0	V	
I_{DD}	Output Amplifier Drain Supply Current		6.9	12.5	mA	
V_{PG}	Photogate Bias Voltage	6.5	7.0	7.5	V	
V_T	DC Electrode Bias Boltage	4.5	5.0	5.5	V	Note 2
V_{EI}	Electrical Input Bias Voltage		11.4		V	Note 3
V_{SS}	Substrate (Ground)		0.0		V	

AC CHARACTERISTICS: (Note 1)
T_P = 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter. All operating voltages nominal specified values.

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range					
	(relative to peak-to-peak noise)	250:1	500:1			Note 9
	(relative to rms noise)	1250:1	2500:1			
NEE	RMS Noise Equivalent Exposure		0.0002		μJ/cm²	Note 10
SE	Saturation Exposure		0.4		μJ/cm²	Note 11
CTE	Charge Transfer Efficiency		0.999995			Note 12
V_O	Output DC Level	3.0	5.5	10.0	V	
Z	Output Impedance		1.4	3.0	kΩ	
P	On-Chip Power Dissipation					
	Clock Drivers		90	150	mW	
	Amplifiers		90	150	mW	
N	Peak-to-Peak Noise		2.0		mV	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi TL}$	Transport Clock LOW	0.0	0.3	0.5	V	Notes 4, 5
$V_{\phi TH}$	Transport Clock HIGH	9.75	10.0	10.5	V	Note 5
$V_{\phi XL}$	Transfer Clock LOW	0.0	0.3	0.5	V	Notes 4, 6
$V_{\phi XH}$	Transfer Clock HIGH	9.75	10.0	10.5	V	Note 6
$V_{\phi RL}$	Reset Clock LOW	0.0	0.3	0.5	V	Note 7
$V_{\phi RH}$	Reset Clock HIGH	9.75	10.0	10.5	V	Note 7
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Data Rate)	1.0	2.0		MHz	Note 8

PERFORMANCE CHARACTERISTICS: (Note 1)
T_P = 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter. All operating voltages nominal specified values.

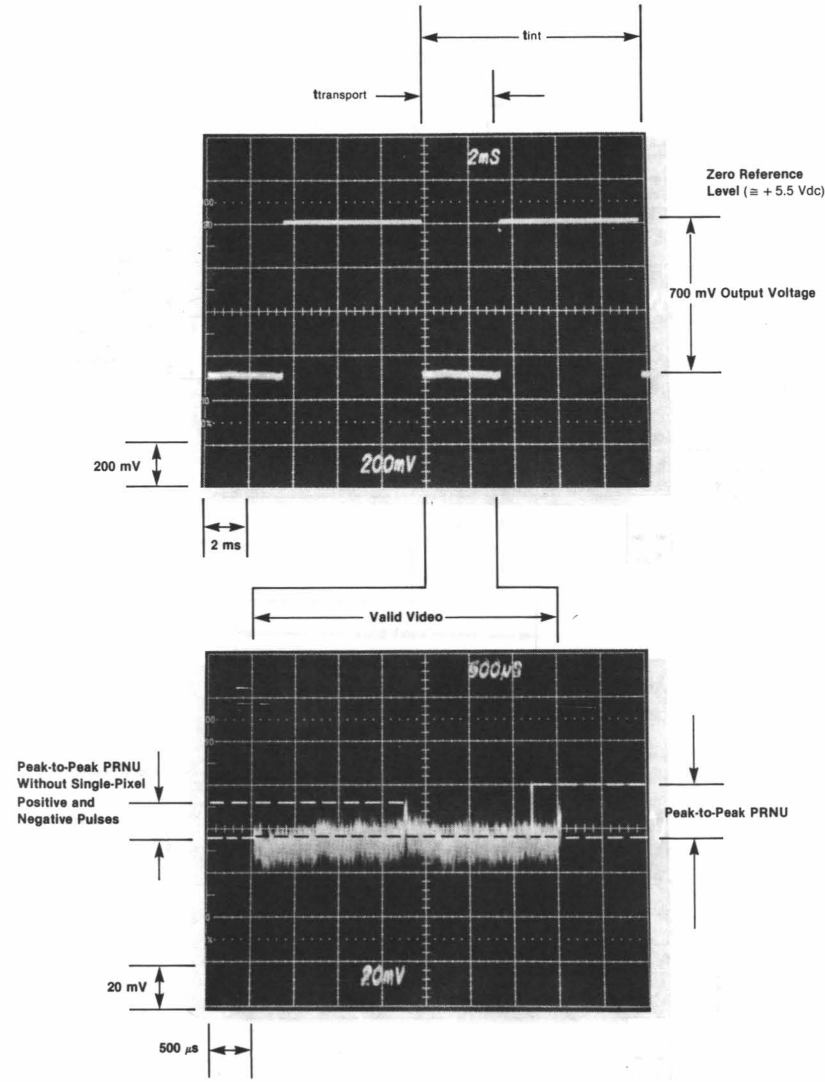
SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-uniformity					
	Peak-to-Peak		160	210	mV	Note 16
	Peak-to-Peak without Single-Pixel Positive and Negative Pulses		100		mV	Note 16
	Single-pixel Positive Pulses		85		mV	Note 16
	Single-pixel Negative Pulses		130		mV	Note 16
	Register Imbalance ("Odd"/"Even")		20		mV	Note 16
DS	Dark Signal					
	DC Component		5	15	mV	Notes 13, 14
	Low Frequency Component		5	10	mV	Notes 13, 14
SPDSNU	Single-pixel DS Non-uniformity		20	40	mV	Notes 13, 15
R	Responsivity	2.0	3.5	5.0	Volts per $\mu j/cm^2$	Note 17
V_{SAT}	Saturation Output Voltage	800	1400	1600	mV	Note 18

*All PRNU Measurements taken at a 700 mV output level using an f/2.8 lens and excluded the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the f number increases, the resulting more highly columnated light causes the package window aberrations to dominate and increase PRNU. A lower f number results in less columnated light causing device photosite blemishes to dominate the PRNU.

NOTES:

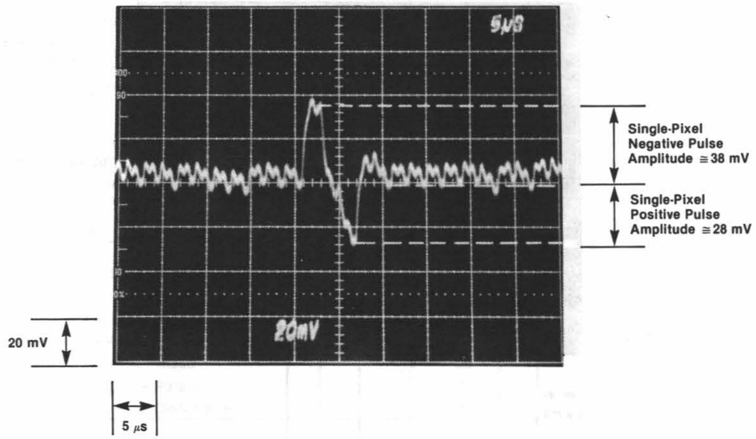
1. T_P is defined as the package temperature.
2. V_T should be equal to (1/2) $V_{\phi TH}$.
3. V_{EI} is used to generate the end-of-scan output and the white reference output. These two signals can be eliminated by connecting V_{EI} to a voltage level equal to $V_{\phi XH}$ + 5 V.
4. Negative transients on any clock pin going below 0.0 V may cause charge-injection which results in an increase of apparent DS.
5. $C_{\phi T} \cong$ 700 pF
6. $C_{\phi X} \cong$ 300 pF
7. $C_{\phi R} \cong$ 5 pF
8. Minimum clock frequency is limited by increase in dark signal.
9. Dynamic range is defined as V_{SAT}/peak-to-peak (temporal) or V_{SAT}/rms noise.
10. 1 $\mu j/cm^2$ = 0.02 fcs at 2854°K, 1 fcs = 50 $\mu j/cm^2$ at 2854°K.
11. SE for 2854°K for light without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 0.8 $\mu j/cm^2$.
12. CTE is the measurement for a one-stage transfer.
13. See photographs for DS definitions.
14. Dark signal component approximately doubles for every 5°C increase in T_P.
15. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in T_P.
16. See photographs for PRNU definitions.
17. Responsivity for 2854°K light source without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 2 V per $\mu j/cm^2$.
18. See test load configurations.

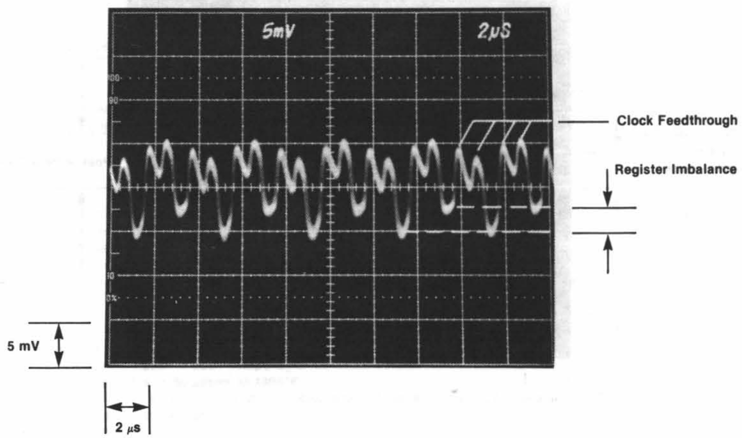
PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS
$T_P \cong$ +25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

PRNU PARAMETERS (CONTINUED)

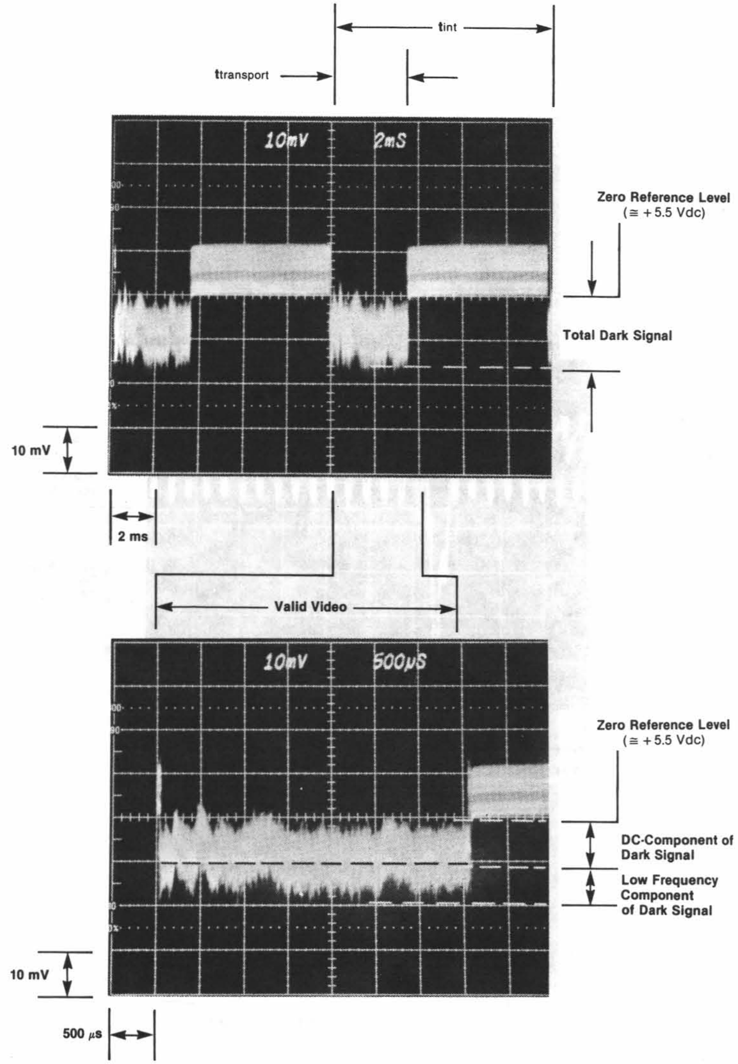




TEST CONDITIONS

TP ≅ +25°C, fφR = 0.5 MHz, tint = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

DARK SIGNAL PARAMETERS (DS)

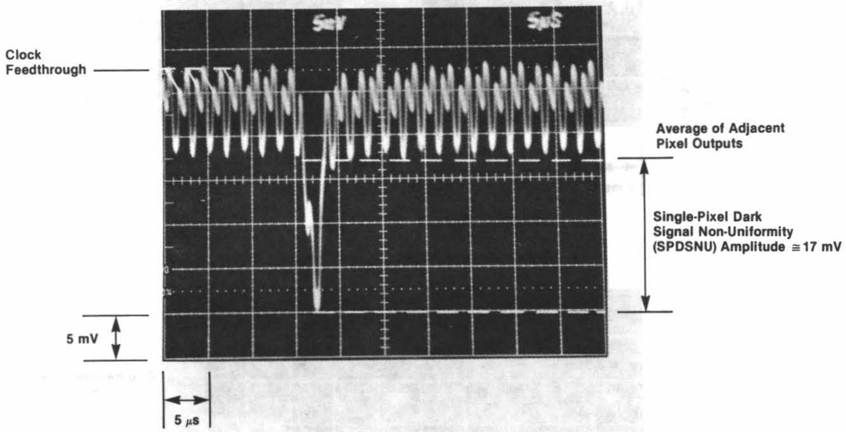


TEST CONDITIONS

TP ≅ +25°C, fφR = 0.5 MHz, tint = 10.0 ms, all voltages nominal specified values.

CCD122/142

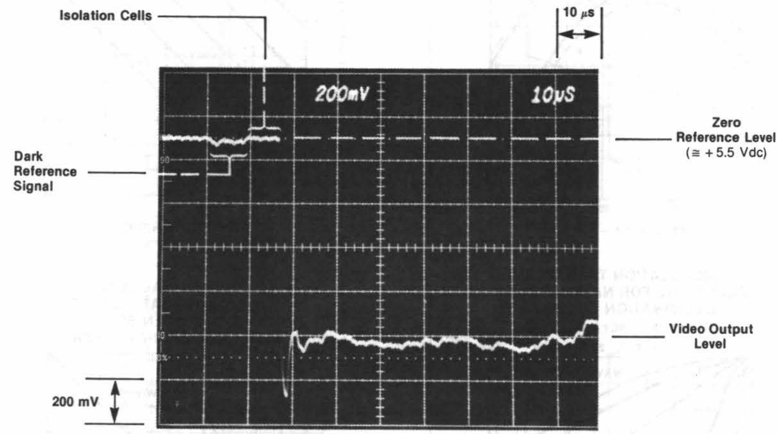
DS PARAMETERS (CONTINUED)



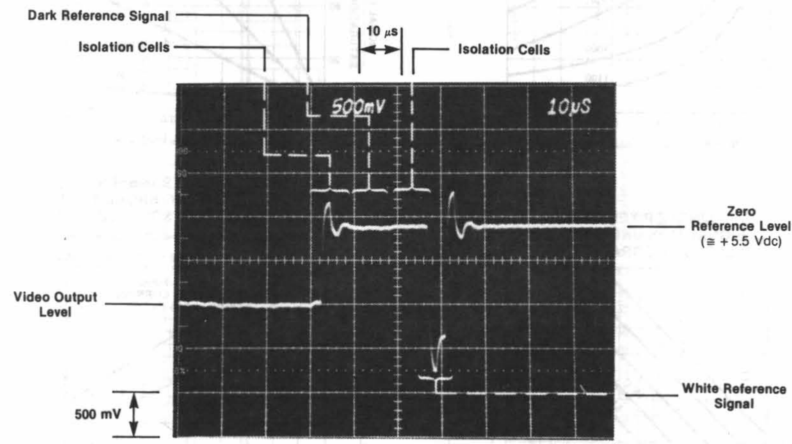
TEST CONDITIONS
TP ≅ +25°C, fφR = 0.5 MHz, tint = 10.0 ms, all voltages nominal specified values.

CCD122/142

VIDEO OUPUT TIMING PHOTOGRAPHS



START OF ONE SCAN VIDEO OUTPUT



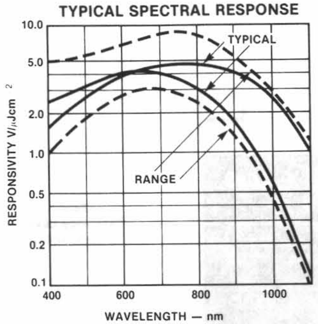
END OF ONE SCAN VIDEO OUTPUT

TEST CONDITIONS
TP ≅ +25°C, fφR = 0.5 MHz, tint = 10 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

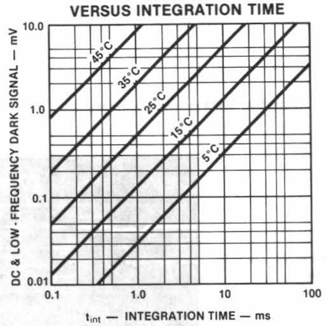
CCD122/142

TYPICAL PERFORMANCE CURVES

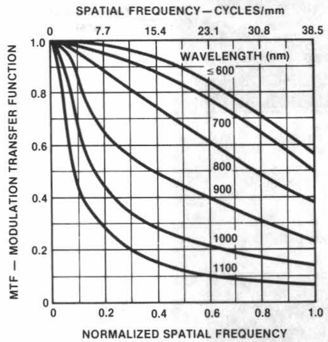
TYPICAL SPECTRAL RESPONSE



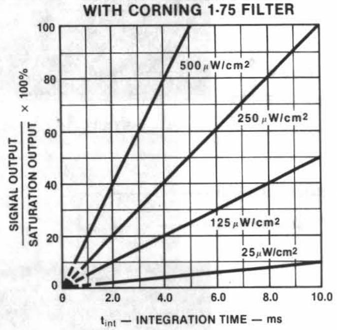
DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME



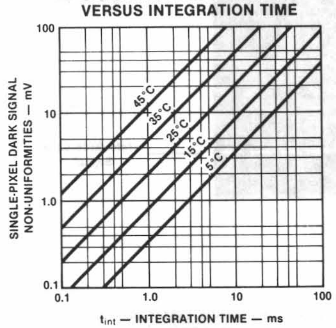
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



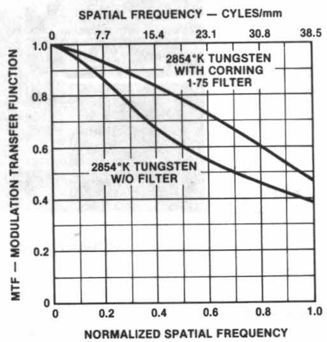
OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH CORNING 1-75 FILTER



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



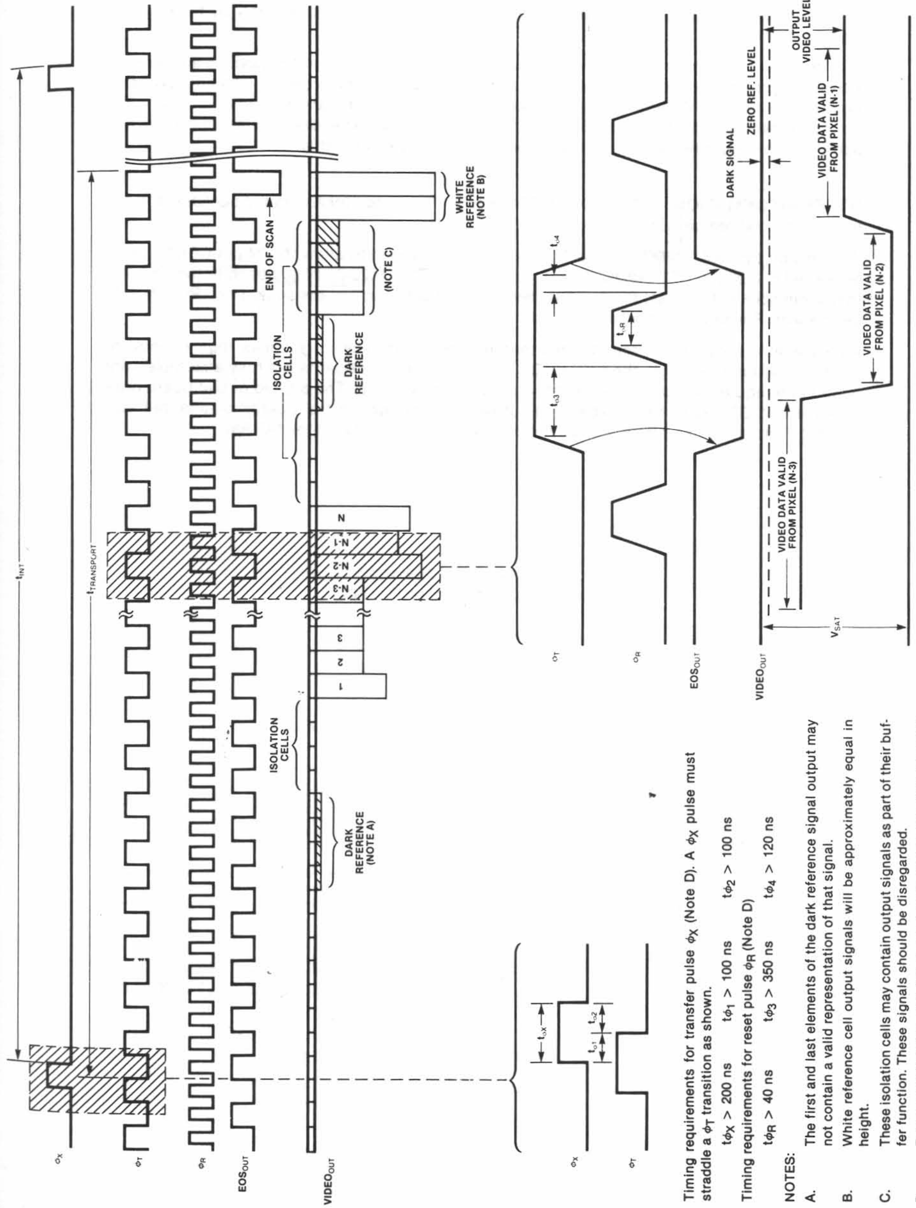
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



The Corning 1-75 filter has the following typical transmittance spectral characteristic: >85% at <600 nm, 60% at 700 nm, 30% at 800 nm, 5% at 900 nm and <2% at >1000 nm.

CCD122/142

TIMING DIAGRAM DRIVE SIGNALS



Timing requirements for transfer pulse ϕ_X (Note D). A ϕ_X pulse must straddle a ϕ_T transition as shown.

$t\phi_X > 200$ ns $t\phi_1 > 100$ ns $t\phi_2 > 100$ ns

Timing requirements for reset pulse ϕ_R (Note D)

$t\phi_R > 40$ ns $t\phi_3 > 350$ ns $t\phi_4 > 120$ ns

NOTES:

A. The first and last elements of the dark reference signal output may not contain a valid representation of that signal.

B. White reference cell output signals will be approximately equal in height.

C. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.

D. Recommended rise and fall times for all clocks are that they are ≥20 ns.

DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

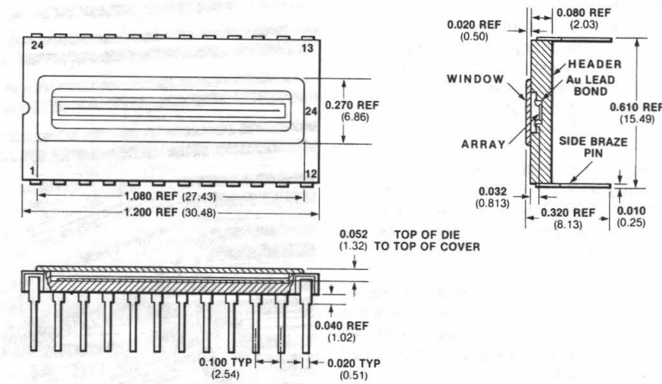
It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION — Order CCD122DC where "D" stands for a ceramic package and "C" for commercial temperature range.

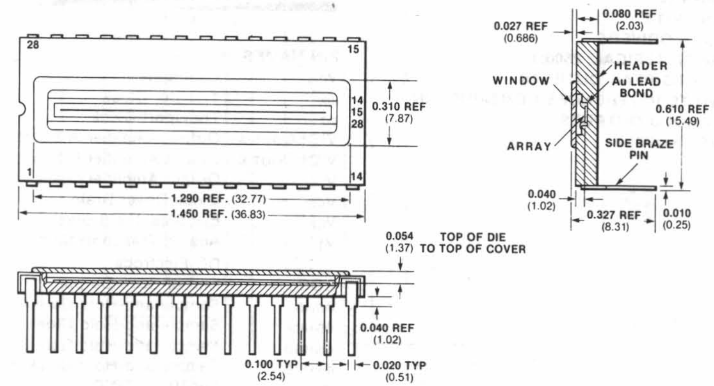
The pins on the CCD122DC and the CCD142DC are arranged to allow the 24-pin CCD122DC to be placed in a 28-pin CCD142DC socket. To do so, the CCD122DC is positioned in the center of the 28-pin socket such that Pin 1 of the device aligns with Pin 2 of the socket and Pin 12 of the device with Pin 13 of the socket.

Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD122DC or CCD142DC. The boards are fully assembled and tested and require only one power supply for operation (+15 V). The printed circuit board order codes are: CCD122DB, CCD142DB. For further information on the boards please call your nearest Fairchild sales office. For any technical assistance, call (415) 493-8001.

CCD122DC PACKAGE OUTLINE
24-Pin Dual In-line Ceramic Package



CCD142DC PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES:

All dimensions in inches (bold) and millimeters (parenthesis). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

CCD133/143

1024/2048-ELEMENT HIGH-SPEED LINEAR IMAGE SENSOR

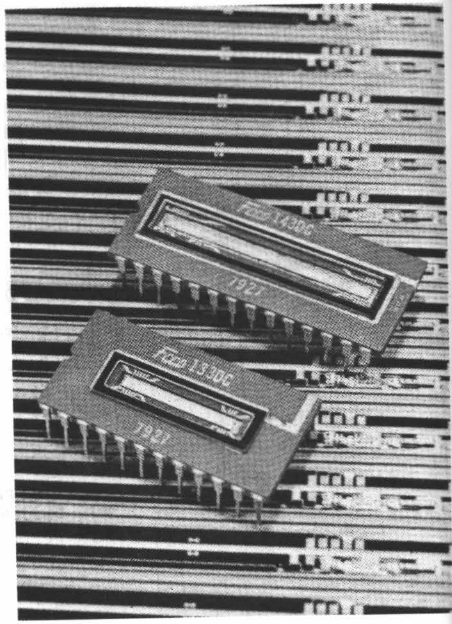
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION

The CCD133 and CCD143 are 1024 and 2048-element line image sensors, respectively. The charge-coupled devices are designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolution, high sensitivity, and high data rates.

The 1024 sensing elements of the CCD133 provide a 120-line per inch resolution across an 8 1/2-inch page and the 2048 sensing elements of the CCD143 an 8-line per millimeter resolution across a 256-millimeter page adopted as the Japanese facsimile standard.

The CCD133 and the CCD143 are second generation devices having an overall improved performance compared with the first generation devices including higher sensitivity, an enhanced blue response and a lower dark signal. The devices also incorporate on-chip clock driver circuitry and are capable of high-speed operation up to a 20 MHz data rate. The photoelement size is 13 μm (0.51 mils) by 13 μm (0.51 mils) on 13 μm (0.51 mils) centers. The devices are manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

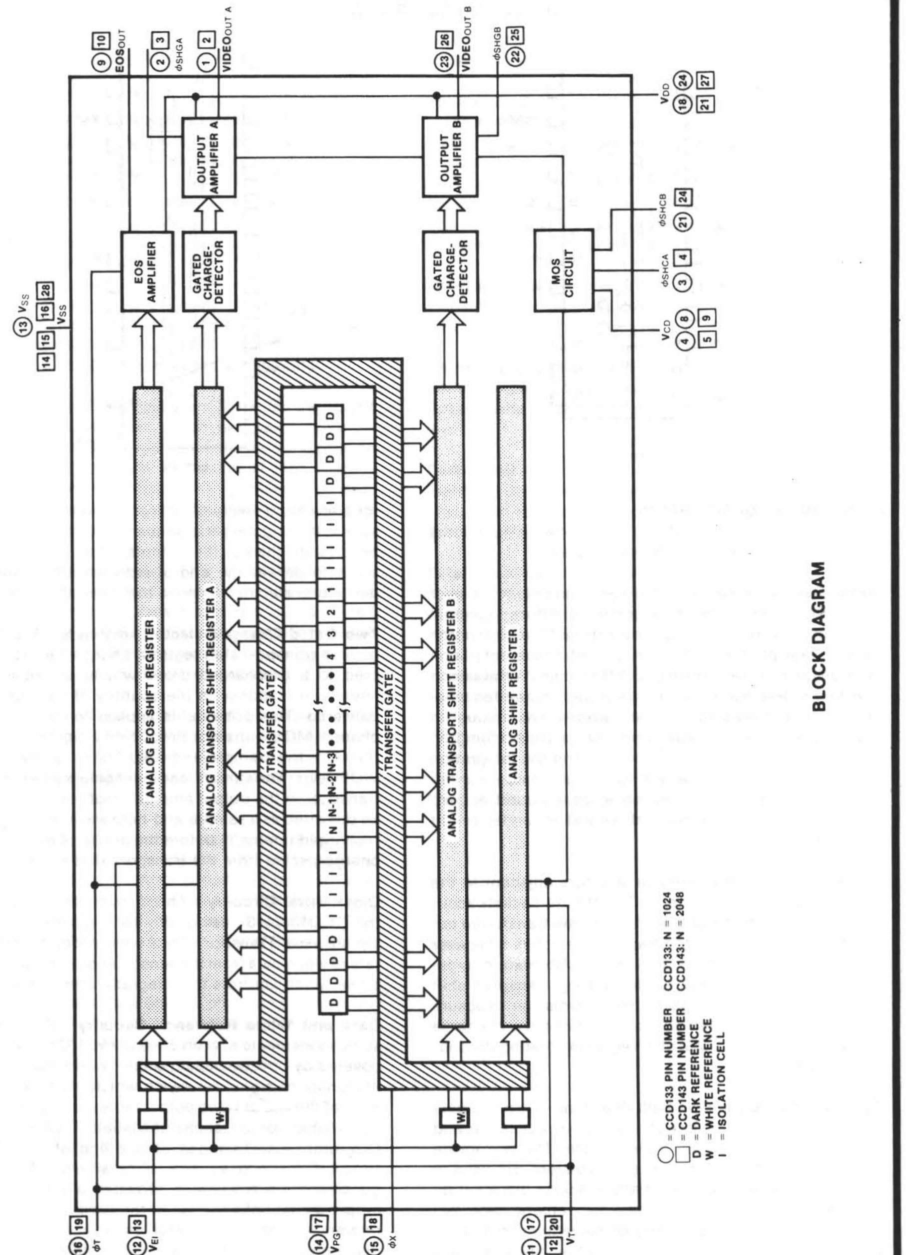


- **HIGH SPEED: UP TO 20 MHz DATA RATE**
- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1 V PEAK-TO-PEAK OUTPUTS**
- **DARK AND WHITE REFERENCES CONTAINED IN SAMPLE-AND-HOLD OUTPUTS**
- **SINGLE POWER SUPPLY**

DB 265.00
DC 357.00

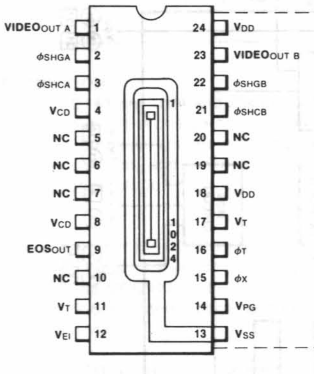
PIN NAMES

V_{PG}	Photogate
ϕX	Transfer Clock
ϕT	Transport Clock
$VIDEO_{OUT\ A}$	Output Amplifier A Source
$VIDEO_{OUT\ B}$	Output Amplifier B Source
V_{DD}	Output Amplifier Drain
V_{CD}	Clock Driver Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
EOS_{OUT}	End-of-Scan Output
$\phi SHGA$	Sample-and-Hold Gate A
$\phi SHCA$	Sample-and-Hold Clock A
$\phi SHGB$	Sample-and-Hold Gate B
$\phi SHCB$	Sample-and-Hold Clock B
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

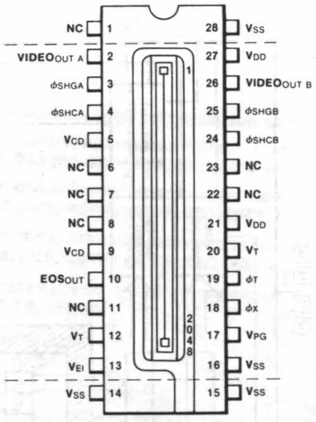


BLOCK DIAGRAM

CONNECTION DIAGRAM DIP (TOP VIEW)



CCD133



CCD143

FUNCTIONAL DESCRIPTION

The CCD133/143 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements —These are elements of a line of 1024/2048 image sensors separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate —This gate is a structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements and permits entry of charge to the End-of-Scan (EOS) shift registers creating the end-of-scan waveform.

Four 529/1041-Bit Analog Shift Registers —Two registers are on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the two charge-detector/amplifiers. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of charge-packets to the amplifiers so that the original serial sequence of the line of video may be reestablished at the outputs. The outer two registers serve to deliver the end-of-scan waveform and reduce peripheral electron noise in the inner shift registers.

Two Gated Charge-Detector/Amplifiers —From the end of each transport shift register, charge-packets are delivered to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-hold waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Clock Driver Circuitry —This circuitry allows operation of the CCD133/143 using only two external clocks, (1) a square wave Transport Clock which controls the readout rate of video data from the sensor, and (2) a Transfer Clock pulse which controls the integration time of the sensor.

Dark and White Reference Circuitry —Four additional sensing elements at both ends of the 1024/2048 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the 1024/2048 illuminated sensor elements (labeled "D" in the Block Diagram). Also included at one end of the 1024/2048 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labeled "W" in the Block Diagram). These reference levels are useful as inputs to external dc restoration and/or automatic gain control circuitry.

DEFINITION OF TERMS

Charge-Coupled Device —A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X —The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T —The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifiers.

Gated Charge-Detector/Amplifiers —These are the output circuits of the CCD133/143 which receive the charge-packets from the CCD transport shift registers and provide a signal voltage proportional to the size of each charge-packet received. Before each new charge-packet is sensed, an internal reset clock returns the charge-detector voltages to a fixed base level.

Sample-and-Hold Clock ϕ_{SHC} —This is an internally supplied voltage waveform applied to the sample-and-hold gate in the amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting ϕ_{SHGA} and ϕ_{SHGB} to V_{DD} and leaving pins ϕ_{SHCA} and ϕ_{SHCB} unconnected.

Dark Reference —Video output level generated from sensing elements covered with opaque metalization provides a reference voltage equivalent to device operation in the dark. This permits use of external dc restoration circuitry.

White Reference —Video output level generated by on-chip circuitry provides a reference voltage permitting external automatic gain control circuitry to be used. The reference voltage is produced by charge-injection under the control of the electrical input bias voltage (V_{EI}). The amplitude of the reference is typically 70% of the saturation output voltage.

Isolation Cell —This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark and white reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range —The dynamic range is the saturation exposure divided by the peak-to-peak noise equivalent exposure. (This does not take into account any dark signal components.) Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

Peak-to-Peak Noise Equivalent Exposure —This is the exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure —Saturation exposure is the minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency —This is the percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range —This is the spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity —Responsivity is the output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal —This is the output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

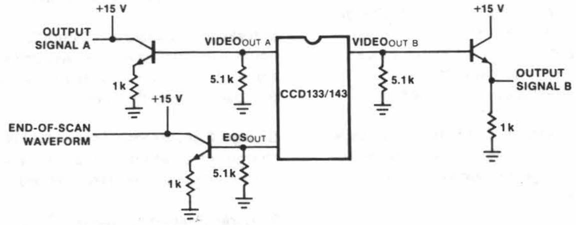
Total Photoresponse Non-Uniformity —This is the difference in the responsive levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Integration Time —The time interval between the falling edges of any two successive transfer pulses ϕ_X is the integration time shown in the Timing Diagram. The integration time is the time allowed for the photosites to collect charge.

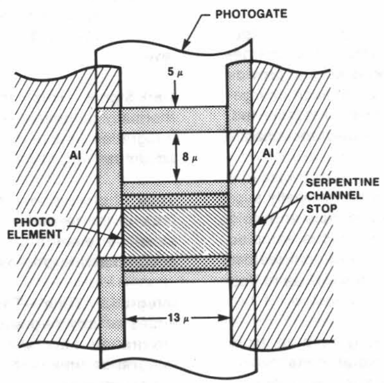
Pixel —This is a picture element (photosite).

CCD133/143

TEST LOAD CONFIGURATION



PHOTOELEMENT DIMENSIONS



All dimensions are typical values.

CCD133/143

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature		-25°C to +125°C
Operating Temperature (See curves)		-25°C to +70°C
CCD133:	Pins 2, 3, 4, 8, 11, 12, 14, 15, 16, 17, 18, 21, 22, 24	-0.3 V to 18 V
	Pin 13	0 V
	Pins 1, 5, 6, 7, 9, 10, 19, 20, 23	NC
CCD143:	Pins 3, 4, 5, 9, 12, 13, 17, 18, 19, 20, 21, 24, 25, 27	-0.3 V to 18 V
	Pins 14, 15, 16, 28	0 V
	Pins 1, 2, 6, 7, 8, 10, 11, 22, 23, 26	NC

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ A&B and EOS_{OUT} to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Notes 1, 2)

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
V_{CD}	Clock Driver Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Clock Driver Drain Supply Current		7.0	15	mA	
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Output Amplifier Drain Supply Current		15	25	mA	
V_{PG}	Photogate Bias Voltage	8.5	9.0	9.5	V	
V_T	DC Electrode Bias Voltage	5.5	6.0	6.5	V	Note 4
V_{EI}	Electrical Input Bias Voltage		10.5		V	Note 5
V_{SS}	Substrate (Ground)		0.0		V	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	CONDITIONS
$V_{\phi XL}$, $V_{\phi TL}$	Transfer & Transport Clock LOW	0.0	0.3	0.5	V	Notes 6, 7
$V_{\phi XH}$, $V_{\phi TH}$	Transfer & Transport Clock HIGH	11	11.5	12	V	Note 7
$f_{DATA\ MAX}$	Maximum Output Data Rate	12	20		MHz	Notes 8, 9

NOTES
1. T_P is defined as the package temperature.
2. All V_{SS} pins must be grounded. All V_{DD} pins must be connected and tied to V_{CD}. All NC pins must be left unconnected.
3. $V_{DD} = V_{CD}$.
4. $V_T = 0.55\ V_{\phi XH} = 0.55\ V_{\phi TH}$.
5. V_{EI} is used to generate the end-of-scan output and the white reference output. These two signals can be eliminated by connecting V_{EI} to a voltage level equal to $V_{\phi XH}$ + 5 V.
6. Negative transients on any clock pin going below 0.0 V may cause charge-injection which results in an increase in apparent DS.
7. $C_{\phi T}$ = 350 pF for CCD133, $C_{\phi T}$ = 700 pF for CCD143, $C_{\phi X}$ = 150 pF for CCD133, $C_{\phi X}$ = 300 pF for CCD143.
8. Minimum clock frequency is limited by increase in dark signal.
9. $f_{DATA} = 2 \times f\ \phi_T$.
10. Dynamic range is defined as V_{SAT}/peak-to-peak temporal noise or V_{SAT}/rms temporal noise.
11. 1μj/cm² = 0.02 fcs at 2854°K, 1 fcs = 50 μj/cm² at 2854°K.
12. SE for 2854°K broadband light without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 0.8 μj/cm².
13. CTE is the measurement for a one-stage transfer.
14. See photographs for PRNU definitions.
15. Video mismatch is the difference in ac amplitudes between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
16. DC mismatch is the difference in dc output level (V_O) between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$.
17. See photographs for DS definitions.
18. Dark signal component approximately doubles for every 5°C increase in T_P.
19. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in T_P.
20. Responsivity for 2854°K broadband light source without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 2 V per μj/cm².
21. See test load configurations.

CCD133/143

AC CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)	500:1 2500:1	1000:1 5000:1			Note 10
NEE	RMS Noise Equivalent Exposure		0.00013		μj/cm2	Note 11
SE	Saturation Exposure		0.67		μj/cm2	Note 12
CTE	Charge Transfer Efficiency		0.99999			Note 13
V_O	Output DC Level	4.0	8.0	11.0	V	
Z	Output Impedance		0.75	1.5	kΩ	
P	On-Chip Power Dissipation Clock Drivers Amplifiers		 100 170	 215 325	 mW mW	
N	Peak-to-Peak Temporal Noise		2.0		mV	

PERFORMANCE CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

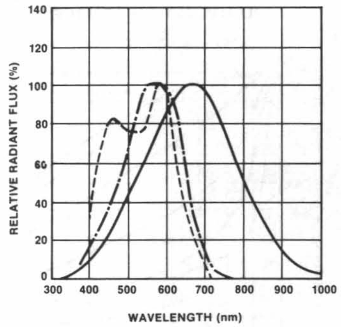
SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU**	Photoresponse Non-Uniformity:					Note 14
	Peak-to-Peak		180	240	mV	
	Peak-to-Peak Without Single-Pixel Positive & Negative Pulses		120		mV	
	Single-Pixel Positive Pulses		100		mV	
	Single-Pixel Negative Pulses		150		mV	
M_{VIDEO}	Video Mismatch		40	160	mV	Note 15
M_{DC}	DC Mismatch		0.5	2.0	V	Note 16
DS	Dark Signal:					Notes 17, 18
	DC Component		2.0	5.0	mV	
	Low Frequency Component		2.0	5.0	mV	
SPDSNU	Single-Pixel DS Non-Uniformity		5.0	20	mV	Notes 17, 19
R	Responsivity	1.8	3.0	4.5	Volts per μj/cm2	Note 20
V_{SAT}	Saturation Output Voltage	1.0	2.0	2.5	V	Note 21

* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror
** PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array. Also excluded from the measurement are video and dc mismatch.
All PRNU measurements are taken at a 800 mV output level using an f/5.0 lens.
The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly columnated light causes the package window aberrations to dominate and increase PRNU. A lower "f" number results in less columnated light causing device photosite blemishes to dominate the PRNU.

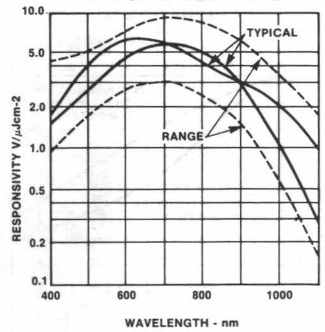
CCD133/143

TYPICAL PERFORMANCE CURVES

***RELATIVE RADIANT FLUX VS WAVELENGTH**

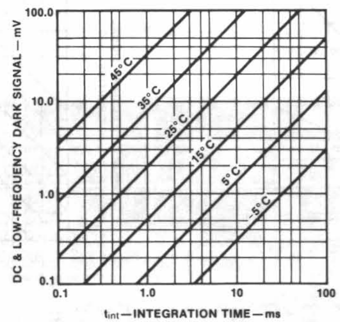


TYPICAL SPECTRAL RESPONSE



— — — TYPICAL "DAYLIGHT FLUORESCENT" BULB
— - — 2854° K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
——— 2854° K LIGHT SOURCE + 3.0 mm THICK 1-75

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME

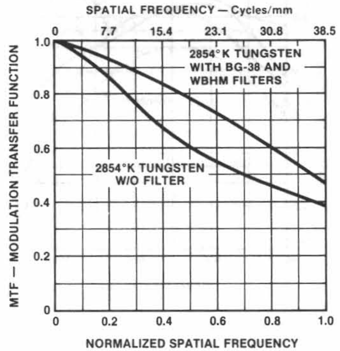


* See note Page 7.

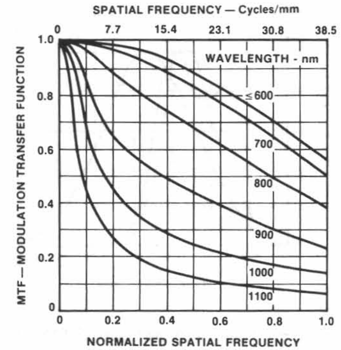
CCD133/143

TYPICAL PERFORMANCE CURVES

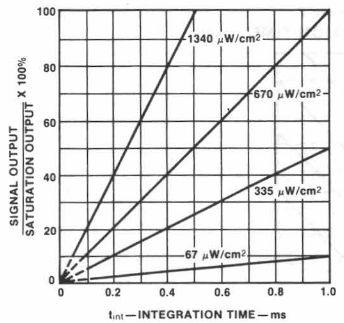
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



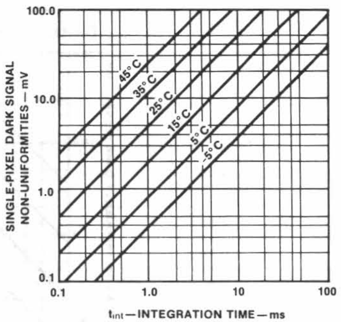
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS

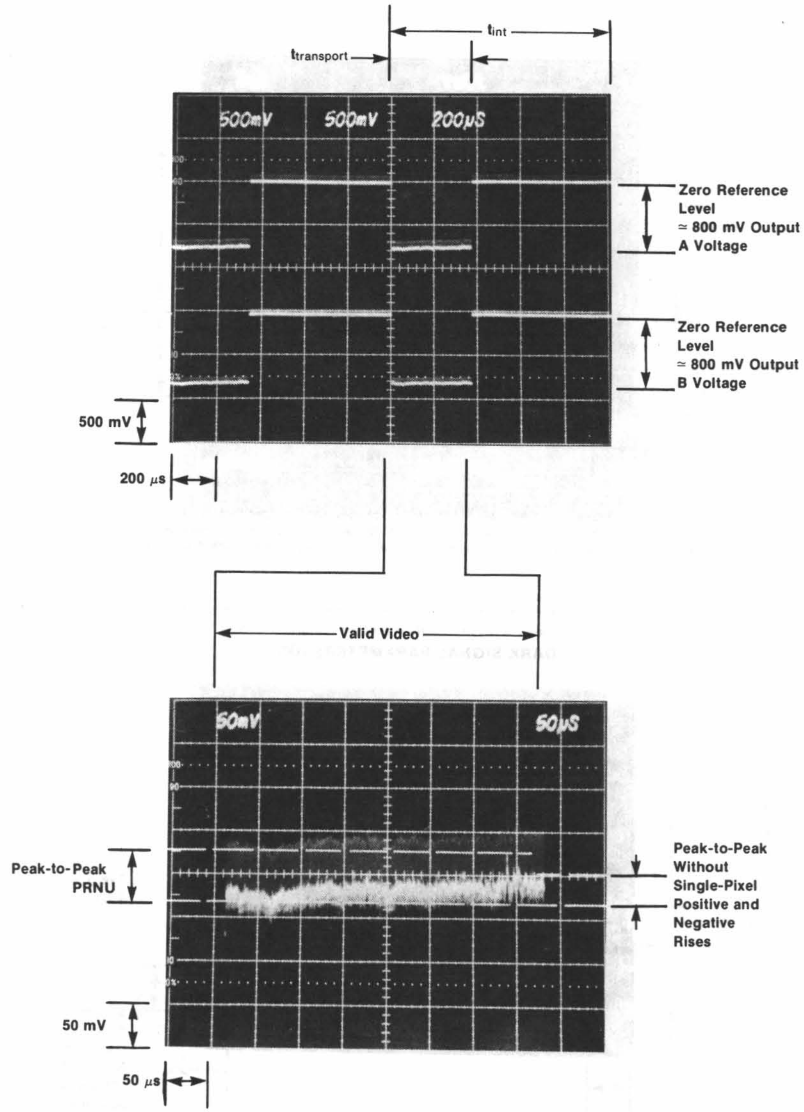


SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



CCD133/143

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS

T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≈ 800 mV. Output fed through 5 MHz low pass filter.

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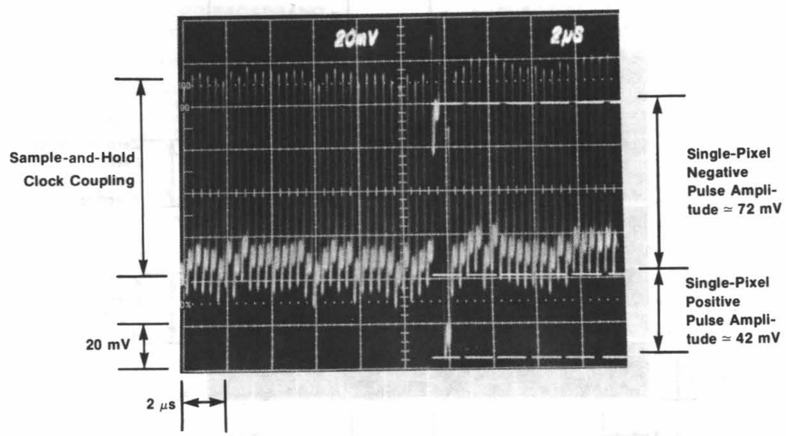
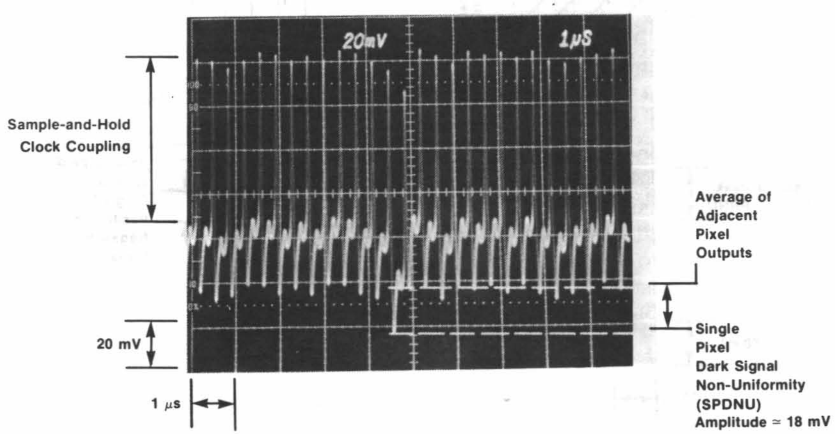


TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≈ 800 mV. Output fed through 5 MHz low pass filter.

DARK SIGNAL PARAMETERS (DS)



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter

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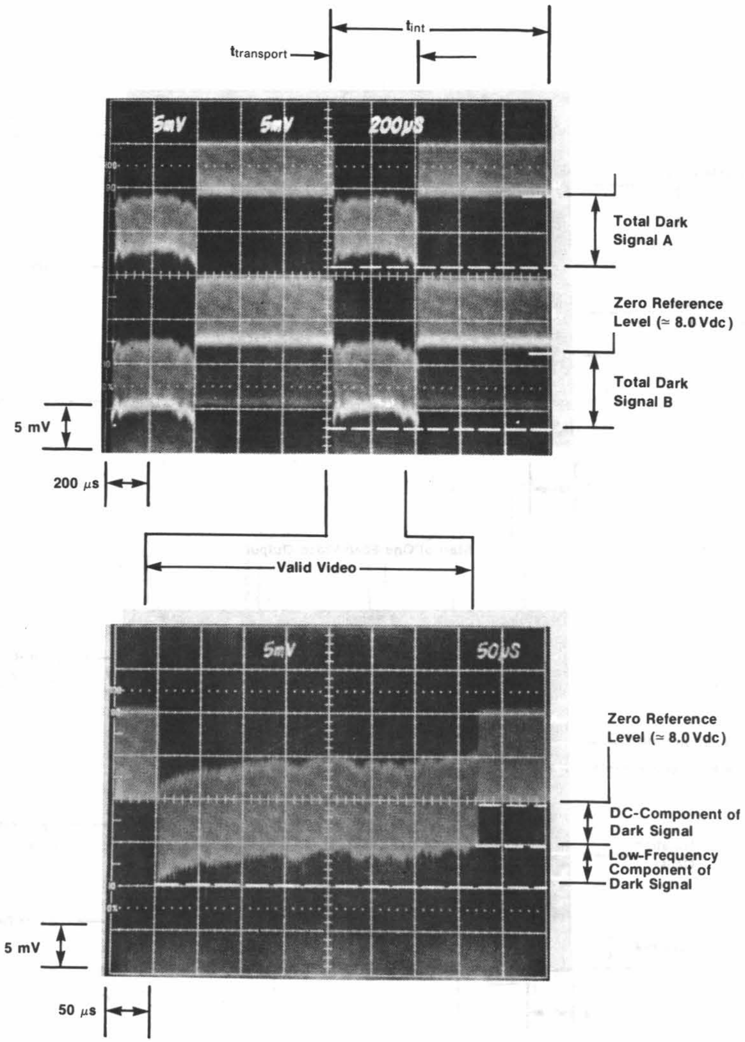
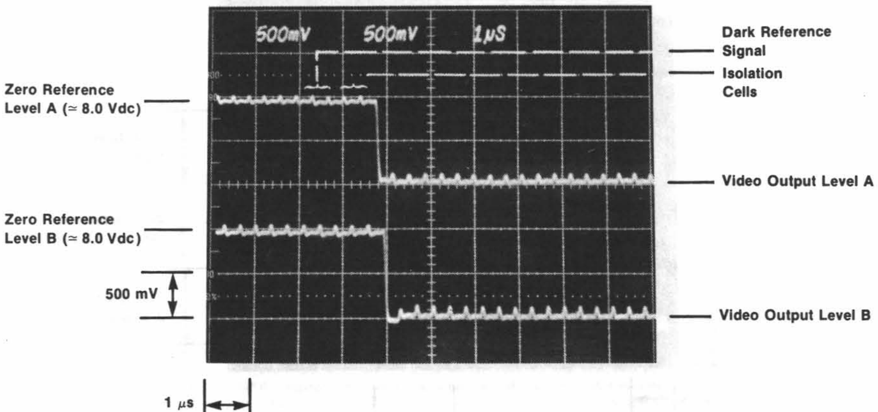
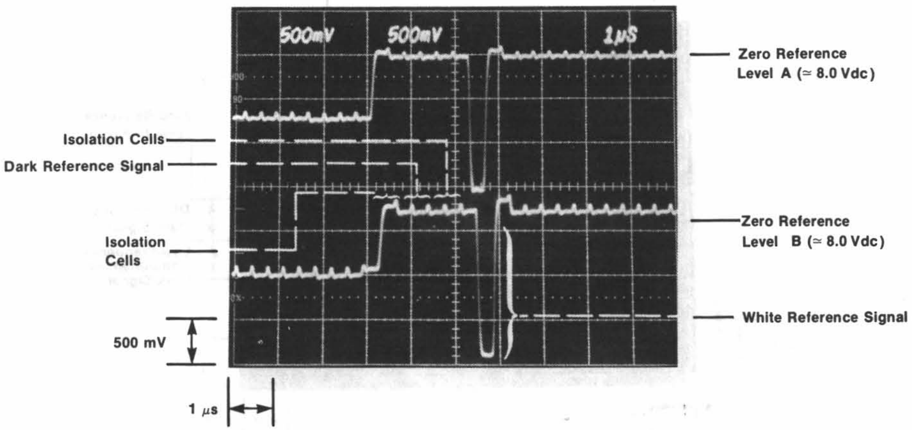


TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

VIDEO OUTPUT TIMING PHOTOGRAPHS



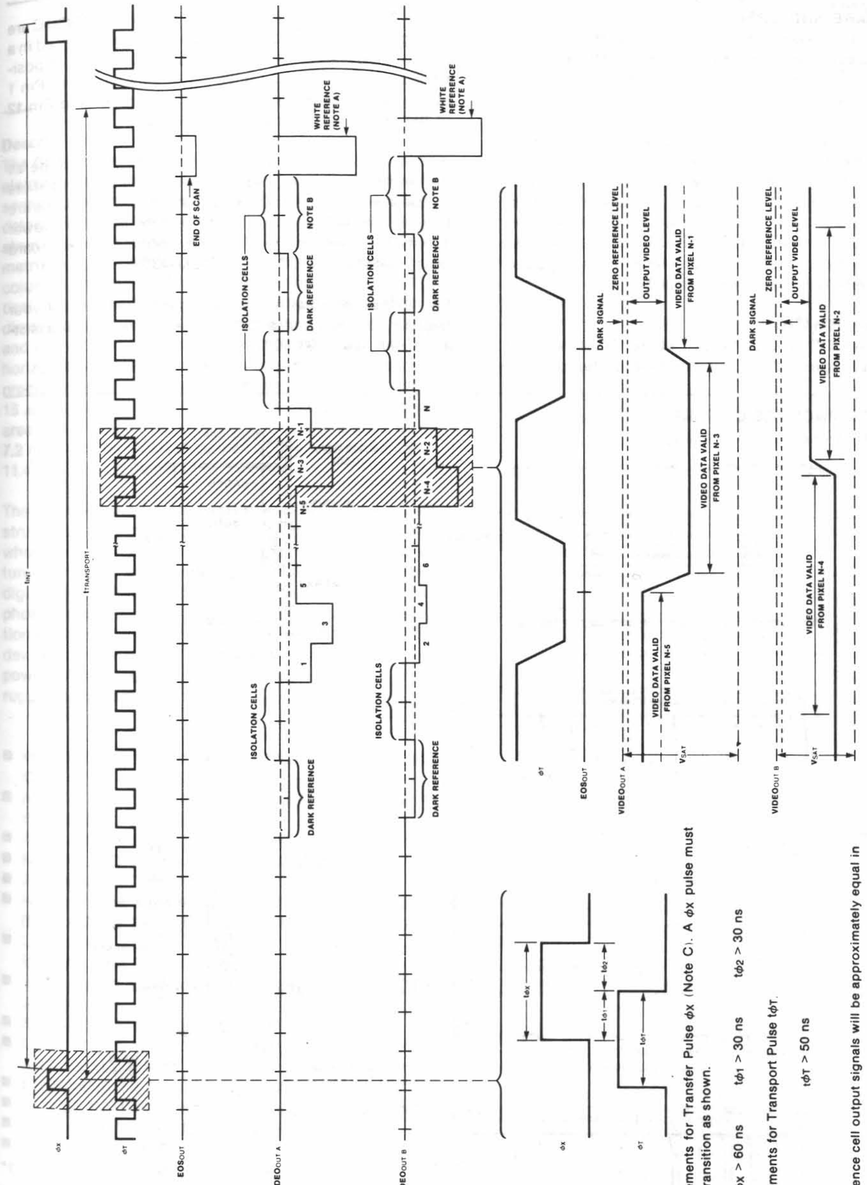
Start of One Scan Video Output



End of One Scan Video Output

TEST CONDITIONS

T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten with 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter



TIMING DIAGRAM

Timing requirements for Transfer Pulse ϕX (Note C). A ϕX pulse must straddle a ϕT transition as shown.

$t_{\phi X} > 60$ ns $\quad t_{\phi 1} > 30$ ns $\quad t_{\phi 2} > 30$ ns

Timing requirements for Transport Pulse $t_{\phi T}$.

$t_{\phi T} > 50$ ns

NOTES:
A. White reference cell output signals will be approximately equal in height.
B. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.
C. Recommended rise and fall times for all clocks are that they are ≥20 ns.

CCD133/143

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

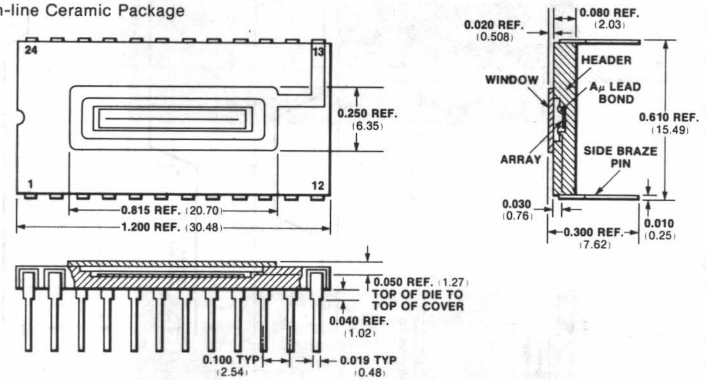
ORDER INFORMATION

Order CCD133DC, or CCD143DC, where "D" stands for a ceramic package and "C" for commercial temperature range. The pins on the CCD133DC and the CCD143DC are arranged to allow the 24-pin CCD133DC to be placed in a 28-pin CCD143DC socket. To do so, CCD133DC is positioned in the center of the 28-pin socket such that Pin 1 of the device aligns with Pin 2 of the socket and Pin 12 of the device with Pin 13 of the socket.

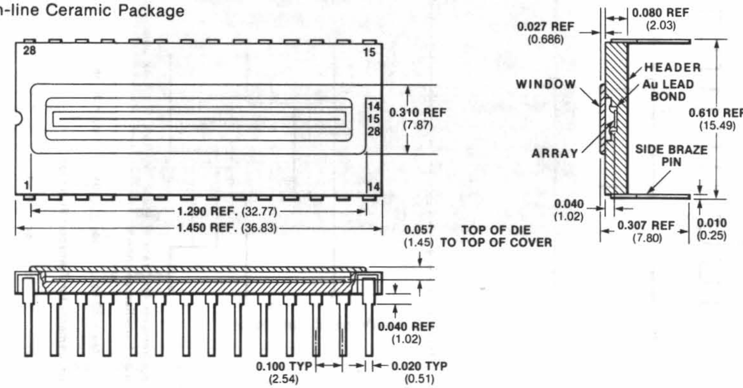
Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD133DC or CCD143DC. The boards are fully assembled and tested and require only one power supply for operation (+20 V). The printed circuit board order codes are: CCD133DB, CCD143DB.

For further information on the boards, please call your nearest Fairchild Sales Office. For any technical assistance, call (415) 493-8001.

CCD133DC PACKAGE OUTLINE
24-Pin Dual In-line Ceramic Package



CCD143DC PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

CCD211
244x190 Element Array
CCD221
488x380 Element Array
CCD Imaging

Description

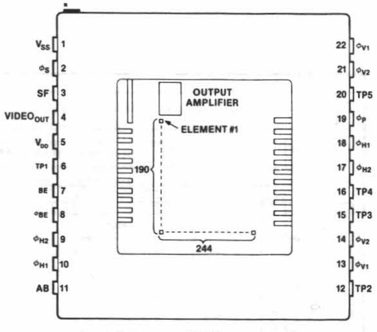
The CCD211 and CCD221 are 244x190 and 488x380-element solid-state charge-coupled device area image sensors which are intended for use as high-resolution detectors in a variety of scientific and industrial optical instrumentation systems. The CCD211 is organized as a matrix array of 244 horizontal lines by 190 vertical columns and the CCD221, 488 horizontal lines by 380 vertical columns of charge-coupled photoelements. The dimensions of the 46,360 photoelements of the CCD211 and the 185,440 photoelements of the CCD221 are 12 μm horizontally by 18 μm vertically. The photoelements are precisely positioned on 30 μm horizontal centers and 18 μm vertical centers. The CCD211 has an image sensing area of 4.4 by 5.7 mm, with a diagonal dimension of 7.2 mm and the CCD221 has an active area of 8.8 by 11.4 mm, with a diagonal of 14.4 mm.

The low noise performance of the buried channel CCD structure can provide excellent low-light-level capabilities when cooled. The geometric accuracy of the device structure, combined with a video readout which is controlled by digital clock signals, allows the signal output from each photo-element to be precisely identified for easy realization of computer-based image processing systems. The devices can be used in video cameras that require low power, small size, high sensitivity, high reliability and rugged construction.

- **46,360/185,440* SENSING ELEMENTS ON A SINGLE CHIP**
- **AVAILABLE HORIZONTAL RESOLUTION: 190/380 ELEMENTS PER LINE**
- **AVAILABLE VERTICAL RESOLUTION: 244/488 LINES**
- **NO LAG, NO GEOMETRIC DISTORTION**
- **A GAMMA OF UNITY**
- **HIGH DYNAMIC RANGE—TYPICALLY: 1,000:1 at 25°C (EXCLUDING DARK SIGNAL NON-UNIFORMITY)**
- **LOW LIGHT LEVEL CAPABILITY, LOW NOISE EQUIVALENT EXPOSURE**
- **VIDEO DATA RATES UP TO 20 MHz, FRAME RATES TO 360/90 Hz**
- **SAMPLE-AND-HOLD VIDEO OUTPUT**
- **LOW POWER DISSIPATION, SOLID-STATE RELIABILITY AND SMALL SIZE**
- **STANDARD TV ASPECT RATIO (4:3)**
- **CCD221 SATISFIES NTSC RESOLUTION STANDARDS**
- **TWO-PHASE REGISTER CLOCKING**
- **DIGITALLY-CONTROLLED READOUT**

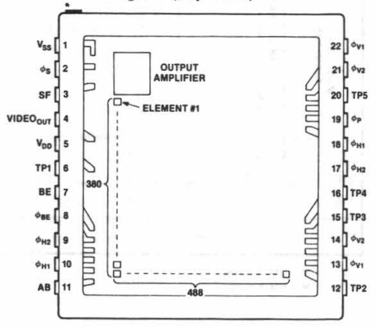
*CCD211 Parameter/CCD221 Parameter

Connection Diagram (Top View)



CCD211

Connection Diagram (Top View)



CCD221

*PIN 1 (V_{SS}) IS DESIGNATED BY A DOT ON SIDE OF PACKAGE

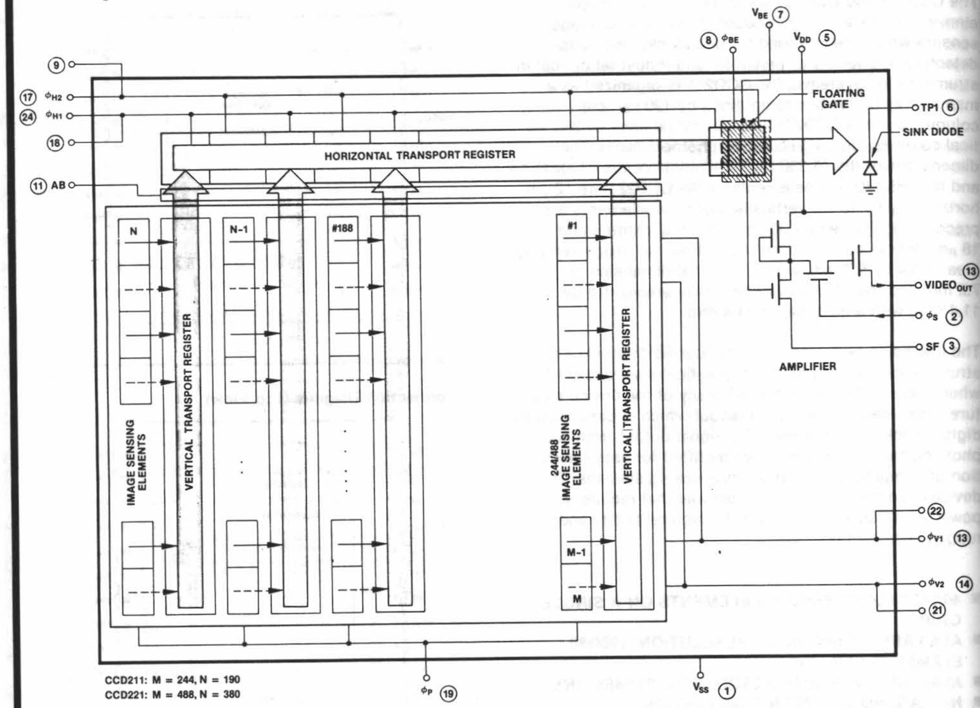
Pin Names

AB	Anti-Blooming Bias (for Column Anti-Blooming)
SF	Floating-Gate Amplifier Source
$VIDEO_{OUT}$	Output Amplifier Source
ϕ_P	Photogate Clock
ϕ_{V1}, ϕ_{V2}	Vertical Transport Clocks
ϕ_{H1}, ϕ_{H2}	Horizontal Transport Clocks
ϕ_{BE}	Bias Electrode Clock
BE	DC Bias Electrode
ϕ_S	Sample-and-Hold Clock
V_{DD}	Output Amplifier Drain
V_{SS}	Substrate (GND)
TP	Test Points

FAIRCHILD
A Schlumberger Company

CCD

Block Diagram



Functional Description
The CCD211/221 consist of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements
Image photons pass through a transparent polycrystalline silicon gate structure and are absorbed in the silicon crystal structure creating hole-electron pairs. The resulting photoelectrons are collected in the photosites during the integration period; the amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and the integration period.

Vertical Analog Transport Registers
At the ends of integration periods, the charge packets are transferred out of the array in two sequential fields of 122/244 lines each. When the photogate voltage is lowered, charge packets from odd-numbered photosites (1, 3, 5 . . . 243/487) are transferred to the vertical transport registers at the beginning of readout of an odd field when the ϕ_{V1} clock is HIGH. Clocking ϕ_{V1} and ϕ_{V2} then transports the charge packets up the vertical transport registers, line by line, to the output horizontal transport register. Before the readout of the next even field and when the photogate voltage is again lowered, the ϕ_{V2} clock is held HIGH causing the transfer of the even-numbered photosite charge packets (2, 4, 6 . . . 244/488) to the vertical registers. A minimum of 123/245 vertical clock pulses are required per field to deliver the entire field to the output. The additional clock cycle is required due to

the existence of a non-sensitive anti-blooming line between the horizontal transport register and the top of the vertical columns.

Horizontal Analog Transport Register
The horizontal transport register is a 190/380 element 2-phase register that receives the charge packets from the vertical registers line by line. After each line of information is transferred from the vertical transport registers, it is moved serially to the output amplifier by the complementary horizontal clocks ϕ_{H1} and ϕ_{H2}. A minimum of 195/385 horizontal clock pulses are required to complete transfer of one line of information to the floating-gate amplifier.

Floating-Gate Amplifier
The charge packets from the horizontal transport register are sensed by a floating-gate whose potential changes linearly with the quantity of signal charge and which drives an input MOS transistor. The output signal from this transistor in turn drives the gate of an output n-channel MOS transistor which produces the video output signal at terminal $VIDEO_{OUT}$. The signal is sampled under control of clock ϕ_S through a MOS transistor switch. The resultant video output signal is a sampled-and-held clock-controlled analog signal representing the spatial distribution of the sensor surface exposure.

Sampled Video Output (SEE TIMING DIAGRAM)
The output waveform of the CCD211/221 is shown in detail in the Timing Diagram. Each *frame* (244/488 horizontal lines) is delivered to the output in two sequential *fields* of 122/244 horizontal lines each. Each horizontal line is 190/380-elements long.

The sequence of data comprising each horizontal line is as follows:
1. At the beginning of each line are 4 pre-scan elements which contain no video information, but are representative of the dark current levels in the horizontal register.
2. The output then contains information from 5 elements which are covered with opaque aluminum including:
   A) A peripheral response element containing information representative of the charge generated around the periphery of the device. This element output should be ignored.
   B) Three dark reference cells which contain no video information, but correspond to the true dark current (the sum of register plus photosite currents) of that particular line. These elemental outputs may be used as dark reference levels in post-output dc restoration circuitry.
   C) A peripheral response reduction element which is partially covered by aluminum.
3. Following are the 185/375 elements which contain the true video information (valid pixels) showing the spatial distribution of incident brightness for that line.

Definition of Terms

Charge-Coupled Device—A charge-coupled device is a monolithic silicon structure in which discrete isolated packets of electrical charge are transported from position to position in the semiconductor by sequential clocking of an array of gates. The charge packets are minority carriers (electrons) with respect to the semiconductor substrate.

Photogate Clock ϕ_P—The voltage waveform applied to the photogate to move the accumulated charge from the image sensor elements to the vertical transport registers.

Vertical Transport Clocks ϕ_{V1}, ϕ_{V2}—The two clocks applied to the vertical transport registers to move the charge packets received from the image sensor elements towards the CCD horizontal transport register.

Horizontal Transport Clocks ϕ_{H1}, ϕ_{H2}—The two clocks applied to the horizontal transport register to move the charge packets received from the vertical transport registers towards the floating-gate amplifier.

Floating-Gate Amplifier—The first stage of the on-chip amplifier which develops a signal voltage linearly proportional to the number of electrons contained in each sensed charge packet. The floating-gate is coupled to the charge transport channel exclusively by electrostatic fields for low-noise signal detection.

Sample-and-Hold Clock ϕ_S—The clock applied to the sample-and-hold gate of the amplifier. The sample-and-hold feature can be disabled by connecting ϕ_S to V_{DD}.

Dark Reference—Video output level generated from photoelements covered with opaque metalization. The video output from these elements provides a reference voltage equivalent to sensor operation in the dark.

Dynamic Range—The saturation level output video signal voltage of the sensor divided by the rms noise output of the sensor in the dark. The peak-to-peak random noise output of the device is 4-6 times the rms noise output.

Saturation Exposure—The minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range—The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

CCD211/CCD221

Responsivity—The output signal voltage per unit exposure for a specified radiation spectrum. Responsivity equals output voltage divided by exposure.

Photoresponse Shading Non-Uniformity—The difference of the response levels between the most and least sensitive regions under uniform illumination, excluding blemished elements. Shading is measured using a low-pass filter with a cut-off of approximately 10 cycles per picture width in the video output line.

Dark Signal—The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

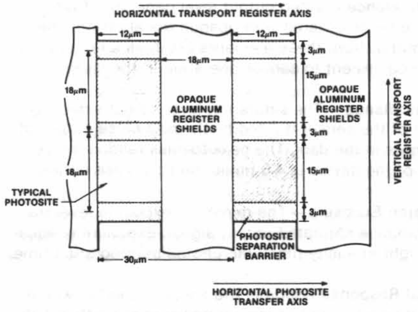
Dark Signal Shading Non-Uniformity—The difference in the dark signal levels between the lowest and highest outputs from non-blemished elements in the dark. Shading is measured using a low-pass filter with a cut-off frequency of approximately 10 cycles per picture width in the video output line.

Saturation Output Voltage—The maximum available useful signal output voltage, measured with respect to the zero reference level.

Integration Time—Two times the time interval between the falling edges of any two successive ϕ_P clock pulses shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel—Picture element (photosite—see dimensions figure 9.)

Photosite Dimensions



NOTE: Photosite Separation Barriers are transparent, photosites are optically contiguous along the vertical axis.

Absolute Maximum Ratings

STORAGE TEMPERATURE	−100°C to +100°C
VOLTAGES:	
Pins 3, 4, 5, 6, 11, 15, 20	−0.3V to +16V
Pins 2, 7, 8, 9, 10, 12, 13, 14, 16, 17, 18, 19, 21, 22	−10V to +15V
Pin 1	V_{SS} = 0V

Caution Note

The devices do not have built-in gate protection. It is crucial that static discharge be controlled and minimized. Care must be taken to avoid shorting pin VIDEO$_{OUT}$ to V_{SS} or V_{DD} during operation of the device. Shorting this pin temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

Dirty glass windows on devices cause increased photoresponse non-uniformity. Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

DC Operating Conditions and Characteristics: Devices are tested at nominal conditions except for V_{SF}, V_{BE}, and V_{AB} which are adjusted for individual sensors.

Symbol	Parameter	Range Min.	Range Nom.	Range Max.	Unit	Remarks
V_{DD}	DC Supply Voltage	12.0	15.0	16.5	V	
V_{AB}	Anti-Blooming Bias Voltage	6.0	10.0	V_{DD}	V	Note 1
V_{SF}	Source of Floating-Gate Amplifier	4.0	7.0	10.0	V	Note 1
V_{BE}	Bias Electrode	-5.0	0.0		V	Note 1
TP_2, TP_4	Test Points		0.0		V	
TP_1, TP_3, TP_5	Test Points		V_{DD}		V	
I_{DD}	DC Supply (V_{DD}) Current		3.5		mA	T_C = 0°C
I_{SF}	Floating-Gate Amplifier Current		1		μA	T_C = 0°C

Clock Conditions

Symbol	Parameter	Range Min.	Range Nom.	Range Max.	Unit	Remarks
$V_{\phi PL}$	Photogate Clock LOW	−6.0	0.0		V	Note 2, 10
$V_{\phi PH}$	Photogate Clock HIGH	3.0	5.0	7.0	V	Note 2
$V_{\phi BEL}$	Bias Electrode of FGA Clock LOW	−3.0	0.0	0.0	V	
$V_{\phi BEH}$	Bias Electrode of FGA Clock HIGH	0.0	5.0	7.0	V	Note 1
$V_{\phi H1L}$, $V_{\phi H2L}$	Horizontal Transport Clock LOW	−5.0	0.0	0.0	V	Note 3
$V_{\phi H1H}$, $V_{\phi H2H}$	Horizontal Transport Clock HIGH	5.0	9.0	12.0	V	Note 1, 3
$V_{\phi V1L}$, $V_{\phi V2L}$	Vertical Transport Clock Low	−6.0	0.0	0.0	V	Note 2, 10
$V_{\phi V1H}$, $V_{\phi V2H}$	Vertical Transport Clock HIGH	5.0	9.0	12.0	V	Note 4
$V_{\phi SL}$	Sample-and-Hold Clock LOW	−3.0	0.0	0.0		
$V_{\phi SH}$	Sample-and-Hold Clock HIGH	3.0	5.0	7.0	V	
$f_{\phi H1}$, $f_{\phi H2}$	Max Horizontal Transport Clock Frequency	7.2		20.0	MHz	Note 5

Performance Specifications: Standard Test conditions are TV format data output at a 30 Hz frame rate, 60 Hz field rate, 15.75 kHz line rate, 7.16 MHz pixel rate, T_C = 0°C. Light source is 2854°K incandescent with 2.0 mm thick Schott BG-38 IR reject filter.

		CCD211/221				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
V_{SAT}	Saturation Output Voltage	200	700		mVp-p	Note 8
DR	Dynamic Range		1000			See definition of terms
SE	Saturation Exposure		0.28		μJ/cm²	Note 6
R	Responsivity		2.5		V/μJcm⁻²	Note 6
Z	Output Impedance		1000		ohm	
CTF_H	Contrast Transfer Function, Horizontal		75		%	At 190/380 line pairs/ picture width
CTF_V	Contrast Transfer Function, Vertical		70		%	At 244/488 line pairs/ picture height
DSSNU	Dark Signal Shading		1	10	% V_{SAT}	Measured with a 1.5 kHz cutoff low pass filter. Note 8, 9
PRSNU	Photo Response Shading		1	10	% V_{OUT}	Measured at V_{OUT} = 50% V_{SAT} with a 1.5 kHz low pass filter. Note 8

Notes

1. Adjustment is required within the indicated range for optimum operation.
2. $C_{\phi P}$ = 4,000 pF for CCD211; $C_{\phi P}$ = 16,000 pF for CCD221.
3. $C_{\phi H1} = C_{\phi H2}$ = 100 pF for CCD211; $C_{\phi H1} = C_{\phi H2}$ = 200 pF for CCD221.
4. $C_{\phi V1} = C_{\phi V2}$ = 3,000 pF for CCD211; $C_{\phi V1} = C_{\phi V2}$ = 12,000 pF for CCD221.
5. Devices are tested at a clock rate of 7.2 MHz. This gives a standard NTSC rate at 30 frames per second. Higher clock rates are possible. Operation of the device at lower or higher frequencies will not damage the device. Two factors contribute to the fundamental low frequency limit: dark current contributions from the photosites and associated dark current non-uniformities, and dark current contributions in the register which will result in increased average dark signal at the output. The longer the intergration time, the higher the spatial non-uniformities.
6. 1 μJ/cm² = (1 μW – S)/cm²
   1 μW/cm² = 3.5 lux with 2854°K + BG-38 filter.
   1 lux = 0.03 μW/cm² with 2854°K + BG-38 filter.
   Energy is measured *after* the filter.
7. Measured with a 100% contrast bar pattern as a test target. The saturation level is where the video peaks just start to flatten out as the incident illumination is increased.
8. Measurement excludes single point blemishes, line and column defects and outer edge elements on a line or field basis.
9. DSSNU reduces (increases) in magnitude by a factor of 2X for every 7-10° reduction (increment) in chip temperature.
10. Minimum increase DSNU for certain arrays results when the low level for these clock signals is between 0 and –6V with respect to V_{SS}.

Cosmetic Performance Specifications

The CCD211 and CCD221 are each available in three cosmetic quality grades. The CCD211A/CCD221A are very high performance devices which are intended for use in the most demanding industrial and scientific applications. The CCD211B/CCD221B are medium grade devices which can be used in situations where a small number of cosmetic defects can be tolerated. The CCD211C/CCD221C are cost-effective devices intended for those applications where less stringent blemish criteria are permissible, for example, in systems which employ computer-based circuitry for analysis of sensor data.

A CCD211 or CCD221 element is considered to be blemished if it exhibits a spurious output (in comparison to its nearest neighbors) of more than 10% of V_{SAT}. Blemish content is determined in the dark, and at an illumination level of 50% V_{SAT}. Single Point Blemishes (SPB's) and column-oriented blemishes (vertical lines) are sometimes found in CCD211 and CCD221 sensors; horizontal line defects are rarely found because of Fairchild's choice of device structure. SPB and column defect locations are random in the CCD211 and CCD221.

Blemish Specifications for CCD211:

	CCD211A Max	CCD211B Max	CCD211C Max	
Number of Single Point Blemishes (SPB)	10	20	50	
Largest SPB Dimension	3	5	8	contiguous pixels
Number of Column Defects (CD)	0	1	4	
Widest Column Defect Width	0	2	3	adjacent columns

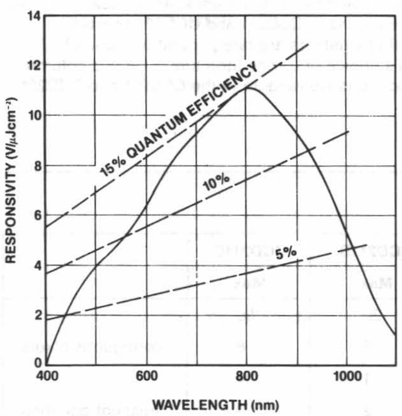
Blemish Specifications for CCD221:

	CCD221A Max	CCD221B Max	CCD221C Max	
Number of Single Point Blemishes	100	200	300	
Largest SPB Dimension	3	5	8	contiguous pixels
Number of Column Defects	4	6	10	
Widest Column Defect Width	2	3	4	adjacent columns
Number of Short Column Defects (SCD)	0	1	2	
Longest SCD Length	0	32	100	lines
Widest SCD Width	0	4	8	columns

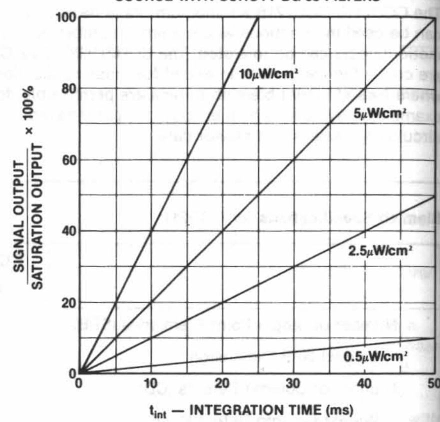
CCD211/CCD221

Typical Performance Curves

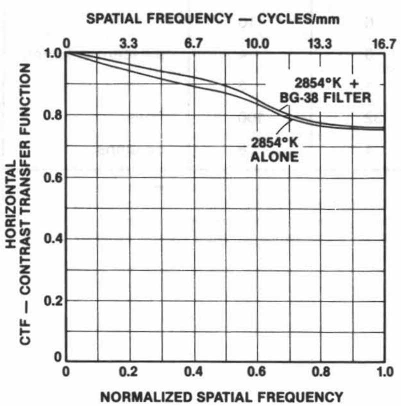
TYPICAL SPECTRAL RESPONSE



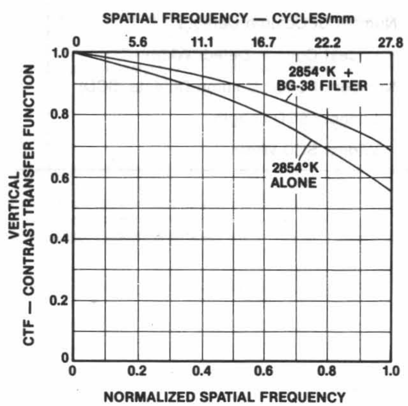
OUTPUT SIGNAL LEVEL VERSUS
INTEGRATION TIME 2854°K TUNGSTEN
SOURCE WITH SCHOTT BG-38 FILTERS



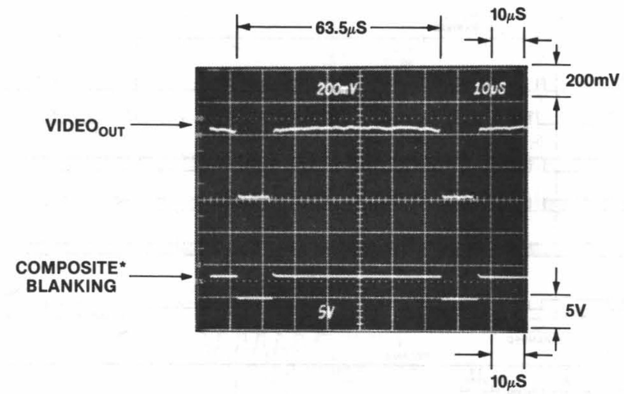
HORIZONTAL CONTRAST
TRANSFER FUNCTION FOR TWO
BROADBAND ILLUMINATION SOURCES



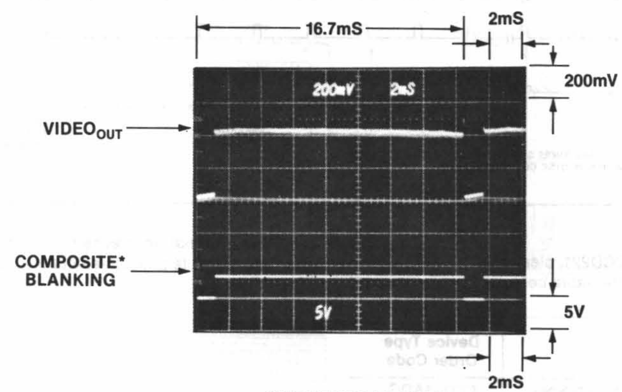
VERTICAL CONTRAST
TRANSFER FUNCTION FOR TWO
BROADBAND ILLUMINATION SOURCES



Output Waveform ($VIDEO_{OUT}$) Under Uniform Illumination ($\approx$ 50% V_{SAT})
Example Shown is for CCD 221



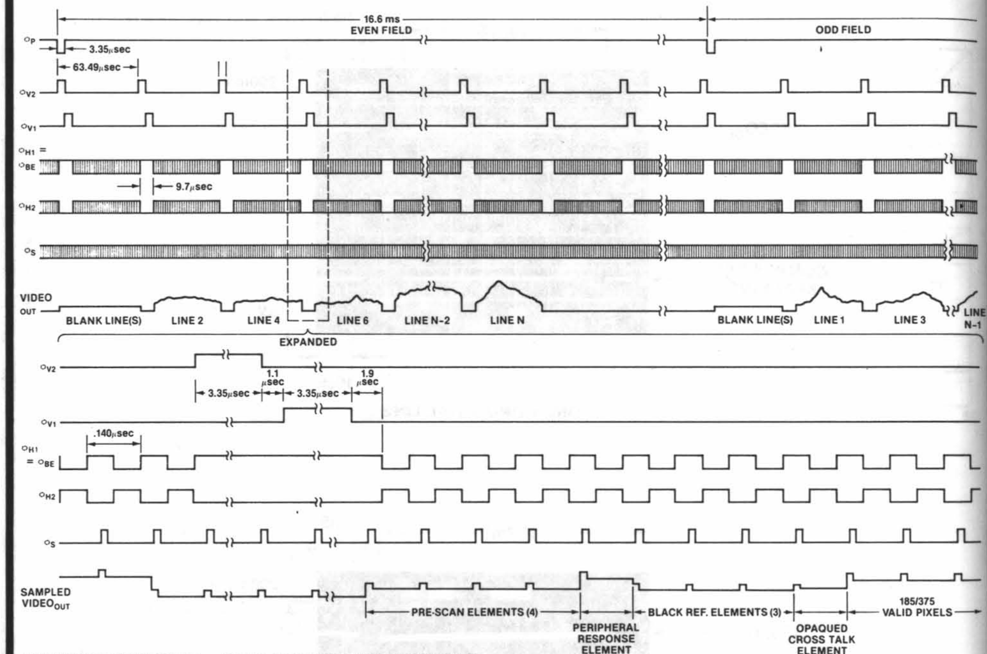
ONE HORIZONTAL LINE



ONE VERTICAL FIELD

*COMPOSITE BLANKING IS GENERATED IN CAMERAS CCD2000C AND CCD2100C

Timing Diagram
CCD211: N = 244
CCD221: N = 488



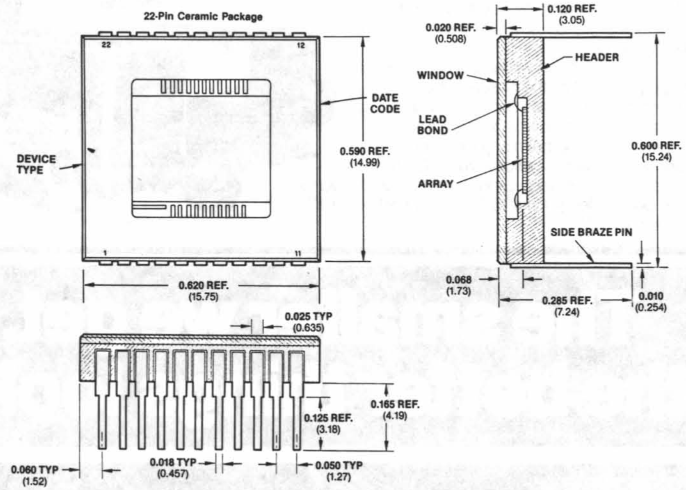
NOTE: DEVICES ARE TESTED AT $f_{\phi R}$ = 7.16MHz. TIMES SHOWN HERE CORRESPOND TO THIS CLOCKING FREQUENCY WHICH IS NTSC COMPATIBLE.

Order Information
To order the CCD211 or CCD221, please follow the ordering codes listed in the table below:

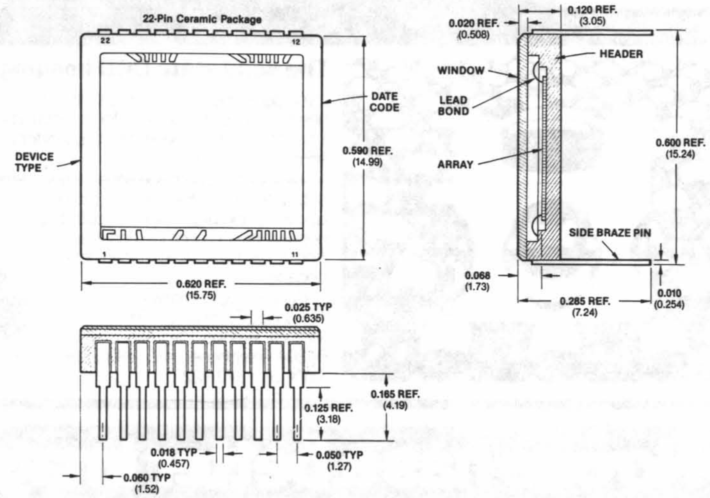
Description	Device Type Order Code
CCD211 Class A Blemish Spec	CD211ADC
CCD211 Class B Blemish Spec	CD211BDC
CCD211 Class C Blemish Spec	CD211CDC
CCD221 Class A Blemish Spec	CD221ADC
CCD221 Class B Blemish Spec	CD221BDC
CCD221 Class C Blemish Spec	CD221CDC

For further information, please call your nearest Fairchild Sales Office. For technical assistance, call (415) 493-8001.

CCD211 Package Outline



CCD221 Package Outline



NOTES: All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement.

CCD Camera Subsystem

Camera Subsystems

Fairchild CCD Camera subsystems are fully assembled and calibrated electro-optical instruments useful in a wide variety of scientific and industrial applications.

Fairchild CCD camera subsystems are ideally suited for computer interfaced system use. Their I/O compatibilities allow operation in response to computer generated signals or asynchronously while providing computer output signals.

The precise geometric accuracy of CCD image sensors make computer processing of optically acquired data practical for many image processing or data analysis applications.

Each camera subsystem includes a camera head which can be supplied with a variety of standard "C" mount lenses, a control unit and associated interconnecting cables.

Camera accessories are available to adapt the basic subsystem to customer requirements.

Line Scan Camera Subsystems

The Fairchild line scan camera subsystems are versatile electronic instruments useful in non-contact optical measurement and data acquisition applications. At the heart of the systems are charge coupled device line scan image sensors providing resolutions of 256, 512, 1024, 1728 or 2048 elements per scanned line. The cameras are used for a wide variety of applications in industrial process controls such as position and size measurements, defect and surface flaw detection as well as general purpose optical recognition of object shapes and sizes.

- Optical resolution up to 2048 elements per scanned line.
- Precise geometric accuracy.
- High-speed data rate up to 10 MHz.
- Exposure time, line scan rate, and video data rate adjustable over wide ranges.
- High sensitivity of CCD sensor permits low light level operation.
- Dynamic range of greater than 200 to 1.
- Solid-state ruggedness and reliability.
- Sample-and-hold video output signal provided.

Applications

The Line Scan camera subsystems find applications in the general areas of non-contact industrial optical inspection and optical data acquisition. The Line Scan Camera subsystems are particularly applicable for use with objects that are generally in motion, i.e., carried by a conveyor mechanism. The precise metric accuracy and digital scanning capability of these subsystems allows easy development of highly sophisticated systems for process and quality control of manufacturing processes.

- Position measurement.
- Size and shape measurement.
- Defect and surface flow detection and categorization.
- Object sorting for size, shape, color or other optically-measureable attributes.
- Gray level detection capability for density measurements.
- General purpose inspection applications.
- BAR code readers for material handling systems.
- Facsimile, OCR, microfiche, and mark-sensing data acquisition.

Specifications

Characteristic	CCD1100C	CCD1200C	CCD1300C	CCD1400C	CCD1500C
Sensor	256x1	512x1	1024x1	1728x1	2048x1
Line Scan Rate	60Hz-35kHz	60Hz-20kHz	60Hz-10kHz	60Hz-6kHz	60Hz-5kHz
Exposure Time	30μs-16ms	51μs-16ms	102μs-16ms	175μs-16ms	204μs-16ms

Data Rate: 100kHz-10MHz, Dynamic Range: $\geq$200:1, Responsivity: 16V/ft cds

Area Camera Subsystems

Fairchild's area camera subsystems are versatile video instruments useful in non-contact optical measurements, optical data acquisition, and television image detection applications. At the heart of the subsystems are Fairchild's CCD area image sensors providing resolutions of 488 by 380 elements and 244 by 190 elements per frame. The cameras can be used for a wide variety of applications in industrial process control and inspection, object location and dimensional measurements, and general purpose television imagery. In addition the camera subsystem provides an excellent introductory vehicle to the capabilities of CCD image sensors.

- High-speed video data rates.
- Low light level operation.
- High dynamic range.
- Low power dissipation.
- Solid state ruggedness and reliability.
- Small size.
- NTSC compatibility.

FAIRCHILD
A Schlumberger Company

CCD

CCD2000C
The CCD2000C, Fairchild's highest resolution area camera subsystem, incorporates the CCD221 area imaging sensor. This array is organized in a 488x380 element format utilizing over 185,000 individual sensing elements per frame. When operated at a 7.16 MHz video data rate, the CCD2000C is fully compatible with NTSC black and white television standards. The CCD2000C can be operated at frame rates up to 60 Hz with external clock signal.

CCD2100C
The CCD2100C uses a 244x190 element array, the CCD211 area imaging sensor. This sensor can provide NTSC resolution over 25% of the area of the TV monitor or it can be used with a non-standard X-Y display monitor. The CCD2100C can be operated at frame rates up to 240 Hz.

Features
The CCD2000 and CCD2100 area camera subsystems are comprised of a system control unit, an interconnecting cable 5′ in length, and a camera enclosure. Interconnecting cables up to 250′ in length can be constructed by the purchaser, or provided by Fairchild upon special request. The control unit contains a 120/240 VAC, 50-400 Hz input power supply, a subsystem timing control card, and pre-wired slots for several available camera performance options. The camera enclosure, which is equipped for dovetail, tripod, or faceplate mounting, contains the CCD driver circuitry and video processing module. Standard C-mount lens can be used with the camera.

The camera provides 1 Vp-p composite video output with negative synch and a ground level black reference voltage from a 75 ohm source impedance. The camera also provides a TTL level binary video output, and a 75 ohm source impedance analog video output directly from the sensor. Camera timing is controlled by differential clock signals provided by the control unit.

The timing circuitry within the control unit develops 30 frames per second, 60 field per second timing control clock sequences required for operation of the CCD sensor and standard NTSC blanking and synchronizing signals in response to an internal crystal controlled oscillator. A TTL external master clock input can be used to achieve scanning rates to 60 frames per second.

The control unit also provides TTL binary video, data rate, sync, blanking and other digital timing output signals which can be useful for construction of digital or analog image processing systems. Addition of the optional ADDBUFF card will provide 18 bit parallel binary coded pixel address outputs; addition of the optional sweep generator card will provide X and Y sweep waveform outputs.

CCD LINE-SCAN CAMERAS MODELS CCD1100, 1300 AND 1400

INCLUDING LENS, CAMERA, CONTROL UNIT, AND INTERCONNECTING CABLE

FEATURES

EASE OF OPERATION

SOLID STATE RELIABILITY

COMPUTER COMPATIBLE
- 0-1 V sample-&-hold video
- Binary video
- Video valid indication
- Internal or external clock control
- Variable exposure time
- Power line synchronized exposure control
- Automatic or fixed gain control

OPTICAL FLEXIBILITY
- Interchangeable C-mount lenses
- Operational without a lens for some applications
- Visible light response
- AGC provides contrast control
- Resolution - 256, 1024 or 1728 elements

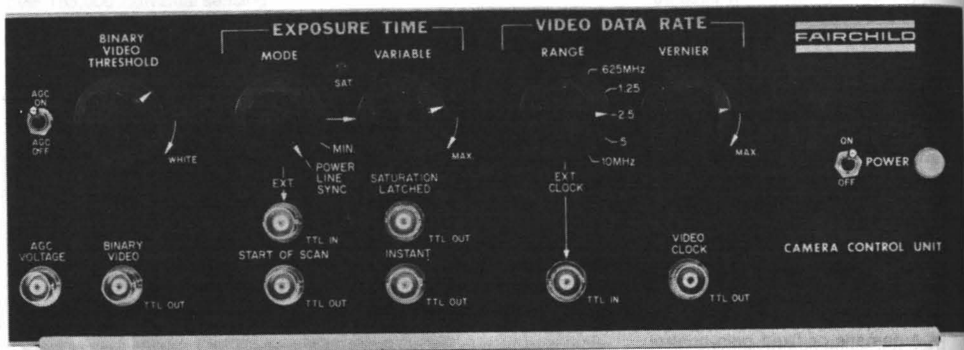
MECHANICAL
- Compact
- Tripod, dovetail, faceplate mountable
- Lightweight

ADVANTAGES OF CCD TECHNOLOGY
- High sensitivity
- Precise photosite spacing
- Low internal operating voltages.

GENERAL DESCRIPTION - The CCD Line Scan Camera is a versatile electronic camera that is easy to operate. A line scan array in the camera senses a line of optical information and produces an analog waveform proportional to the brightness of the image. When motion is applied to the object being sensed, a complete picture or series of line-scan outputs is generated. The system can be used for precision non-contact measurements, facsimile sensing, velocity measurements, surface flaw detection, shape recognition sorting and many other optical sensing functions.

FUNCTIONAL DESCRIPTION - Model CCD1100, CCD1300 and CCD1400 are complete Line-Scan Cameras consisting of a CCD Line-Scan Camera, Control Unit, and interconnecting cable. The subsystem provides all of the necessary control and signal processing functions for realization of a flexible high performance line-scanning camera system. The subsystem permits precise measurement and sensing of optical data. Applications requirements such as document scanning, industrial inspection, surveillance, spectroscopy, microscopy and precision measurements can be satisfied with the subsystem.

LINE SCAN CAMERA - The Line-Scan Camera contains a CCD linear sensor of 256, 1024 or 1728 elements of resolution, a timing control module, a signal processing module and a rugged housing that may be tripod, front faceplate, or dovetail mounted. Selection of a standard lens compatible with the application completes the optical sensing system. A camera to control unit interconnection cable permits complete remote control of the camera by the Control Unit. The Control Unit also accepts input to permit camera control by a microprocessor or computer.



CAMERA CONTROL UNIT - The Camera control Unit, provides four principal operating functions; video output control, video data rate control, exposure control and the camera power supply.

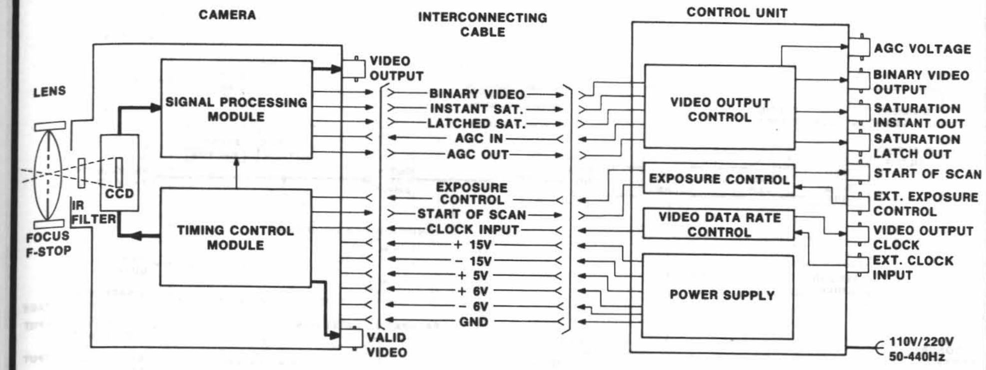
VIDEO OUTPUT CONTROL - A switch selection for automatic gain control or fixed gain is located on the front faceplate. The AGC operating mode is useful for signal compensation due to aging of light source or variations in paper color when scanning facsimile documents. An AGC voltage terminal (BNC) is available for further signal processing. A binary-video threshold adjustment potentiometer controls digital quantizing of the output signal over the complete signal range. A TTL level binary-video output signal is available on the front panel BNC connector.

VIDEO DATA RATE - A video clock oscillator is located in the video data rate section. A 6-position switch and a Vernier potentiometer are also included to permit continuous frequency adjustment from 10 MHz to 100 kHz. An input for externally generated clock pulses can be utilized to synchronize camera operation with an external system.

EXPOSURE CONTROL - The exposure control can operate in two modes: synchronously (under the control of a computer or the control unit), and asynchronously (under the control of the camera). System flexibility is enhanced by these two modes. Another particularly useful feature of the exposure control permits the sensing subsystem to be synchronized with the power line. When utilizing a fluorescent or other ac powered illumination source, no amplitude modulation by the light source appears on the output signal. When the exposure control switch is located in the position marked "variable", an infinite selection of exposure time can be selected. The minimum exposure time is set by the video line rate and the maximum can be adjusted to 16 ms. BNC connectors are available for all incoming and outgoing signals. A light-emitting diode, when on, indicates that the device has saturated. A saturated condition causes no permanent degradation to the sensor or the subsystem.

CAMERA POWER SUPPLY - The control unit can be powered by either a 110 V ac or 220 V ac, 50-440 Hz power line. Switch selection of this option is located on the rear of the unit. A power supply internal to the control unit provides ± 15 V and + 5 V to the camera through the interconnecting cable.

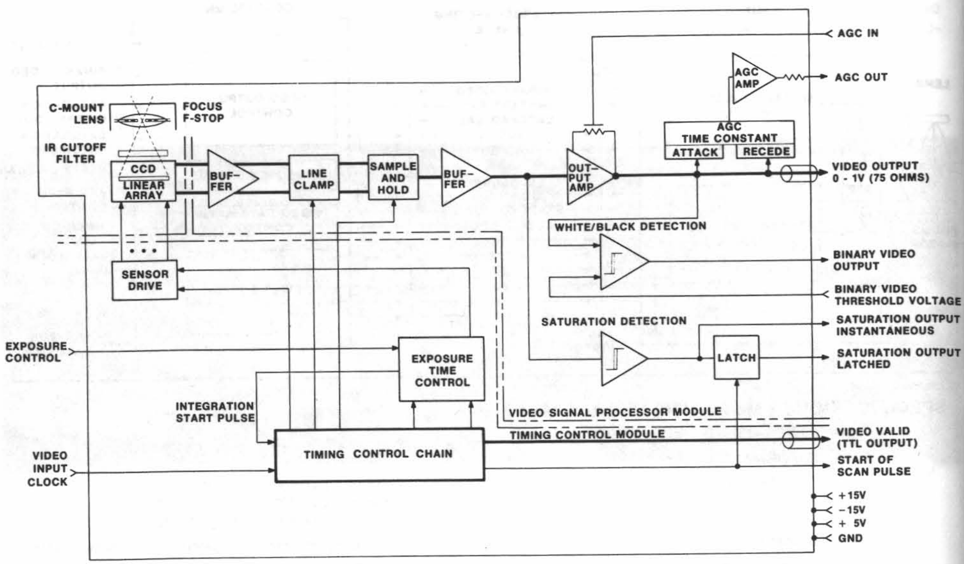
SUBSYSTEM BLOCK DIAGRAM



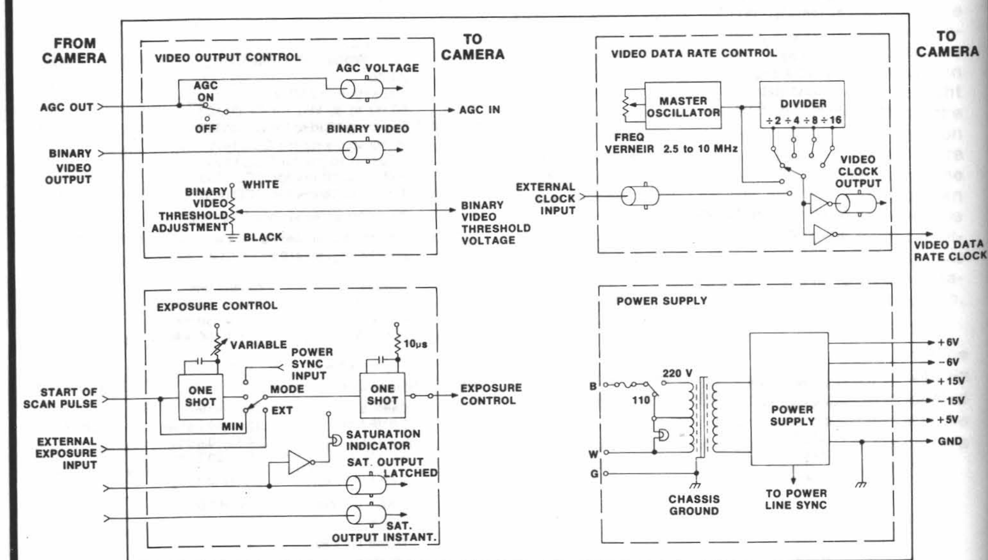
SPECIFICATIONS - Model 1100, 1300 and 1400
Line Scan Camera Subsystem

PERFORMANCE		
Sensor	Model CCD1100: 256×1 CCD110F Model CCD1300: 1024×1 CCD131 Model CCD1400: 1728×1 CCD121H	
Geometric Distortion	System performance is determined by lens selected.	
Dynamic Range	≥200:1	
Responsivity	16 V/ft cd s using a 2854 °K, tungsten source	
Photoresponse Non-Uniformity	± 50 mV measured at 500 mV output level using fixed gain setting	
Saturation Exposure	0.06 ft cd s	
VIDEO OUTPUT		
Analog	$1V_{pp}$ video (75Ω)	
Binary	"1" = White, "0" = Black	
AGC Range	20 db	
Data Rate	100 kHz to 10 MHz	
Line Scan Rate	60 Hz to 35 kHz for CCD1100, 60 Hz to 10 kHz for CCD1300, 60 Hz to 6 kHz for CCD1400	
Exposure Time	30 μs to 16 ms for CCD1100, 102 μs to 16 ms for CCD1300, 175 μs to 16 ms for CCD1400	
SPECTRAL RESPONSE	Approximately visible response	
INPUT POWER	105 - 125 V_{ac} 50-440 Hz 0.1 A 210 - 240 V_{ac} 50-440 Hz 0.05 A	
POWER REQUIREMENTS	Camera +15 V 150 mA −15 V 100 mA + 5 V 350 mA + 6 V 50 mA − 6 V 60 mA	Control Unit +15 V 50 mA −15 V 60 mA + 5 V 100 mA
TEMPERATURE	0 °C to 40 °C	
PHYSICAL DATA Size (without lens)	Camera 2.6" (6.6 cm)	Control Unit 12.0" (30.5 cm)
Width	5.5" (14.0 cm)	4.1" (10.4 cm)
Height	6.0" (15.2 cm)	8.0" (20.3 cm)
Weight	1.7 lbs (0.77 kg)	5.4 lbs (2.45 kg)
Connector	CINCH DB-255 F179 BNC's	CINCH DBC-255 BNC's
Mount	Tripod 1/4 x 20 Dovetail Front Faceplate	

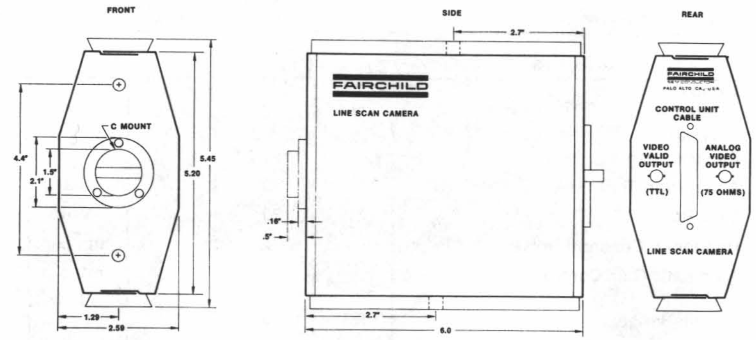
LINE SCAN CAMERA BLOCK DIAGRAM



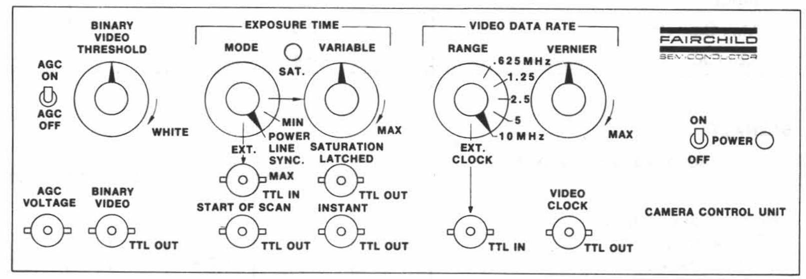
CONTROL UNIT BLOCK DIAGRAM



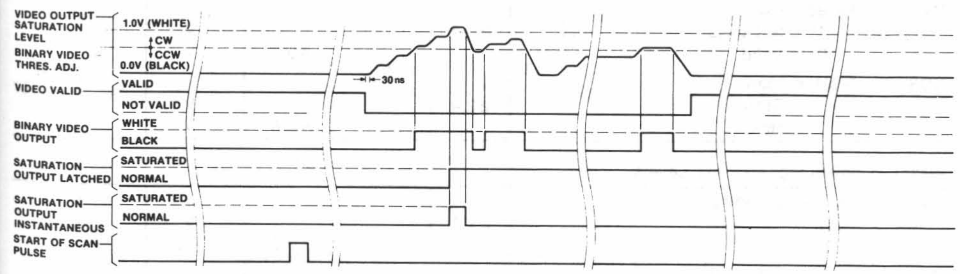
PHYSICAL CONFIGURATION OF LINE SCAN CAMERA



PHYSICAL CONFIGURATION OF CONTROL UNIT



TIMING DIAGRAM LINE SCAN CAMERA SUBSYSTEM



NOTE: EACH VIDEO CLOCK PULSE CORRESPONDS TO A SINGLE PICTURE ELEMENT (PIXEL)

SIGNALS — TO AND FROM THE CAMERA UNIT

ANALOG SIGNALS

SYMBOL	CHARACTERISTICS	RANGE MIN	TYP	MAX	UNITS	DEFINITIONS
OUTPUT — Analog Video Signals						
VO	Video Output					2
	Black		0		V	
	White		1.0		V	
	Dynamic Range		≥200:1			13
	Acquisition Time		30		ns	14
	Slew Rate		20		V/μs	15
	Random & Coherent Noise		5		mV p-p	16
AGCO	Automatic Gain Control Output				mV p-p	9
	Gain Range	9:1	10:1	11:1		
	Max Gain (10:1)		0.6		V	
	Min Gain (1:1)		−4		V	
INPUT - Analog Video Signals						
AGCI	Automatic Gain Control Input					10
	Max Gain (10:1)		0.6		V	
	Min Gain (1:1)		−4		V	

DIGITAL SIGNALS

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	DEFINITIONS
OUTPUT - Digital Video Signals TTL Levels						
BVO	Binary Video Output					1
	"1" = White	≥2.4			V	
	"0" = Black			≤0.8	V	
SOL	Saturation Output Latched					12
	"1" = Saturation	≥2.4			V	
	"0" = Normal			≤0.8	V	
SOI	Saturation Output Instantaneous					11
	"1" = Saturation	≥2.4			V	
	"0" = Normal			≤0.8	V	
VV	Video Valid					4
	"1" = Not Valid	≥2.4			V	
	"0" = Valid			≤0.8	V	
SOS	Start of Scan					5
	"1" = Start	≥2.4			V	
	"0" = Hold			≤0.8	V	
INPUT - Control Signals - TTL Levels						
EC	Exposure Control					8
	"1"	≥2.4			V	
	"0"			≤0.8	V	
VIC	Video Input Clock					7
	Frequency	0.1		10.0	MHz	
	Voltage	≥0.8		≥2.4	V	

LENSES FOR CCD LINE SCAN CAMERA

Lens Focal Length	Maximum Relative Aperture	CCD1100	Angular Field of View CCD1300	CCD1400	Lens Mount
13 mm	F = 1:1.8	16°	60°	91°	C
25 mm	F = 1:1.5	8.5°	33°	54°	C
50 mm	F = 1:1.4	4.2°	17°	28°	C
75 mm	F = 1:3.2	2.8°	11°	19°	C
ZOOM 15 to 150 mm	F = 1:2	14 to 1.4°	53° to 5.6°	82° to 9.5°	C

PARAMETER FOR LENSES OF LINE SCAN CAMERA

OPTICAL CONSIDERATIONS

IMAGE DETECTOR SYSTEM

The image detector utilized by the Line Scan Camera is a monolithic silicon charge-coupled-device structure, which is packaged in a hermetically sealed DIP equipped with an optical-quality glass window.

Sensor Operation

Photo detection in the CCD structure is accomplished in a single row of image sensor elements which are separated by diffused channel stop barriers. The detection mechanism is accumulation of free electrons generated by the photon absorption process. The charge built up in individual photosites is a linear product of the incident illumination intensity and the exposure time over which the electrons are allowed to accumulate.

The charge accumulated within each of the individual photosites is transported sequentially out of the CCD image sensor during a VIDEO VALID scanning line readout period. After further processing, including a sample and hold function, the accumulated charge data becomes the camera's ANALOG VIDEO OUTPUT signal. This signal has an instantaneous amplitude representing the spatial distribution of image brightness along the row of photo detection sites as a function of time. The readout DATA RATE is the subsystem VIDEO CLOCK frequency.

Image detection is a true time integration function: charge is accumulating in each photosite during the total EXPOSURE TIME period which extends from the beginning of one scanning line readout interval until 28 video clock periods preceding the next readout interval. Satisfactory exposures can be made with short flashes from strobe lights or constant-intensity images, depending upon the subject. (Unlike photographic film, the CCD sensor does not suffer any reciprocity failure with very short illumination durations.)

Sensor Geometry

The photo-sensitive area of the image sensor is a row of 256, 1024 or 1728 elements which are on 13 micrometer (0.51 milli-inch) center-to-center spacing. Each sensing site is 13 μ x 13 μ for the CCD1300 and 13 μ x 17 μ for the CCD1100 and CCD1400. The length of the entire photo-sensitive row is 3.3 mm for the CCD1100, 13.3 mm for the CCD1300, and 22.5 mm for the CCD1400. In terms of spatial frequency, the resolution of the image sensor (and therefore of the camera) is 38.4 line pairs per millimeter (lp/mm).

Spectral Response

The spectral response of the Camera has been shaped to a rough approximation of human photopic sensitivity by inclusion of an optical filter glass in the lens holder to decrease infrared sensitivity. This has been shown to give good results in most applications. The filter can be removed, at the purchaser's option, but will result in lower resolution because long-wavelength photons are absorbed deep in the silicon bulk, which leads to inter-element crosstalk.

LENS SELECTION

From a practical viewpoint, selection of a lens for the Line Scan Camera Subsystem is similar to selection of a lens for a photographic camera. Due consideration must be given to the object-to-camera separation, required resolution in the object plane, required depth of focus, available light power density, object size, etc.

Magnification

As used here, "magnification", (M), is defined as the ratio of the object length to the length of the image of the object upon the array. M can be easily derived from the familiar lens equation:

$$\frac{1}{F} = \frac{1}{ID} + \frac{1}{OD}$$

$$M = \frac{OD}{ID} = \frac{OL}{IL}$$

where F = lens focal length, OD = lens-to-object distance (= working distance), ID = lens-to-sensor surface distance at focus, OL = length of object, IL = length of object image upon sensor surface.

Required Illumination

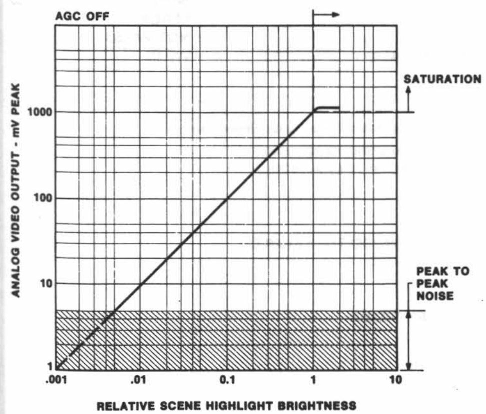
Illumination requirements vary radically, depending upon the camera application. Good results can many times be obtained by use of a power-line driven fluorescent illuminator, and operating the camera in the LINE SYNC exposure control mode. Shorter exposure times will require higher intensity illumination of the object. Either backlighting or frontlighting systems can be used. One way to determine the illumination requirements is to consider the CCD sensor as equivalent to a photographic film with an ASA speed of about 100, and to calculate F-stop and exposure time accordingly.

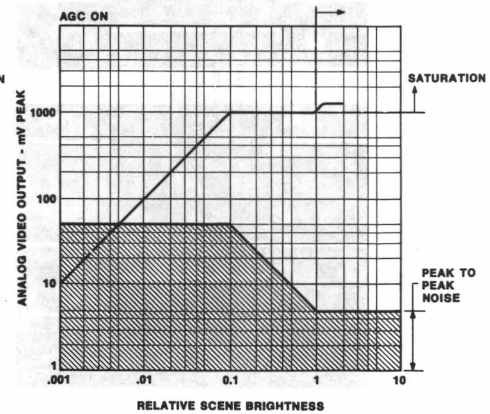
For special help with illumination, such as special filters or light sources, consult the factory at (415) 493-7250.

DEFINITIONS

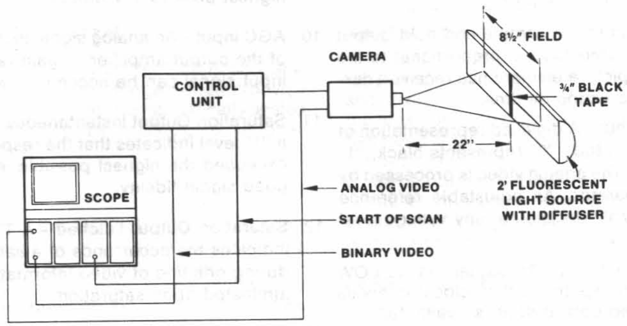
1. Pixel - Picture element. There are 256, 1024 or 1728 pixels in each scanned-line output.
2. Analog Video Output - A sample and hold output waveform whose amplitude is proportional to the light which each picture element has received during the preceding exposure time.
3. Binary Video Output - A digitized representation of the analog video output; "0" represents black, "1" represents white. The analog video is processed by an analog comparator. An adjustable reference level permits "1"/"0" decision at any voltage level between 0 and 1 V.
4. Video Valid Output - A TTL signal that is LOW $\leq$(0.8 V) only during the video clock intervals when actual video data output is available.
5. Start of Scan Output - A TTL signal that can serve as a sync pulse; it goes HIGH for one video clock period immediately preceding the video valid output interval.
6. Video Clock Output - A TTL output signal that indicates the rate at which photosensor element charge packets are being delivered to the output.
7. Video Input Clock - The video output rate of the camera can be controlled by an external clock-generator signal to the external clock input of the control unit.
8. Exposure Time - The amount of time the image sensing elements are allotted to view the image. Control of the exposure time can be synchronized to the camera, synchronized to the control unit (computer or other external source) or synchronized to the power line.
9. AGC Output - An analog signal that represents the magnitude of the gain necessary to amplify the highest pixel to 1 V output.
10. AGC Input - An analog signal that controls the gain of the output amplifier. A gain range of 1X to 10X input signal can be accomplished.
11. Saturation Output Instantaneous - The presence of a "1" level indicates that the respective pixels have exceeded the highest possible level permitted for good signal fidelity.
12. Saturation Output Latched - A TTL indication that indicates the occurrence of a saturation condition during one line of video information. An LED is illuminated upon saturation.
13. Dynamic Range - The analog video output signal level resulting from saturation exposure divided by the peak-to-peak noise content of one video output pixel.
14. Acquisition Time - The time required for the sample and hold circuitry to acquire the associated voltage of next charge packet.
15. Slew Rate - The speed at which the output amplifier can change from the value of one pixel to the value of the next pixel. At a 10 MHz video rate, a full scale output change from one pixel to the next pixel can be accomplished.
16. Random and Coherent Noise - The peak-to-peak noise that appears at the analog video output (excluding dark singal) when no illumination derived signal is present.

SUBSYSTEM CHARACTERISTICS

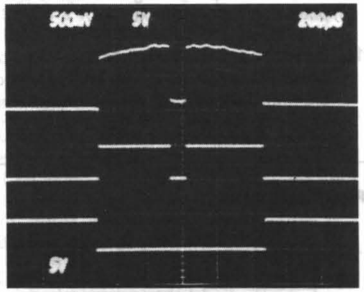




SIMPLE SYSTEM BLOCK DIAGRAM USING CCD1300 SYSTEM



THE FOLLOWING WAVEFORMS WERE TAKEN FROM AN OSCILLOSCOPE WHILE THE CAMERA WAS VIEWING A FLUORESCENT LIGHT FIXTURE WITH A 0.75 INCH BLACK TAPE IN THE MIDDLE.

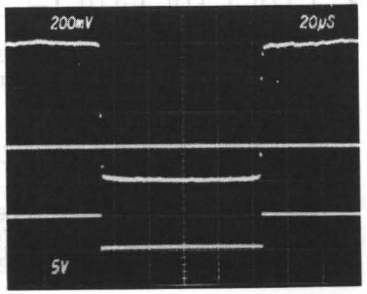


VIDEO OUTPUT

BINARY VIDEO OUTPUT

VIDEO VALID

1 = WHITE
0 = BLACK
1 = NOT VALID
0 = VALID

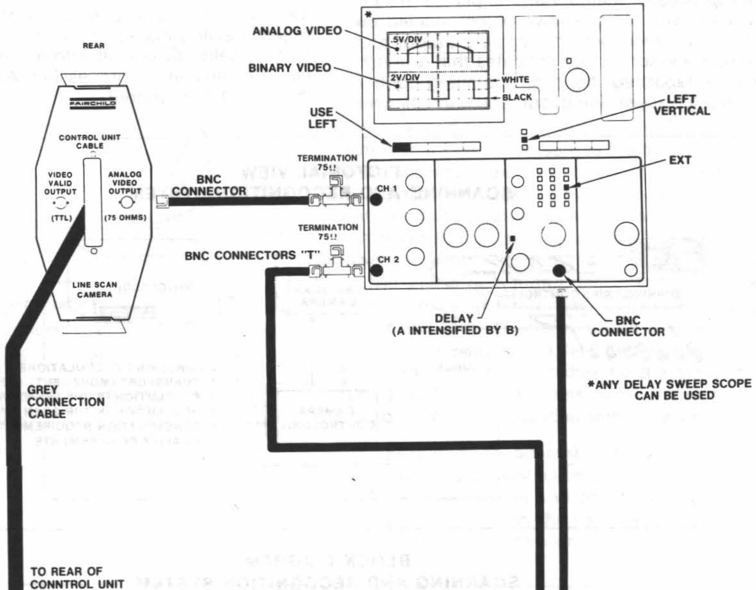


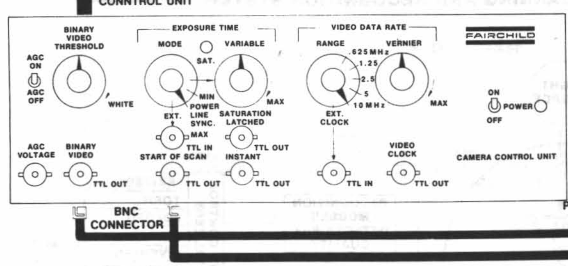
VIDEO OUTPUT EXPANDED

BINARY VIDEO THRESHOLD

BINARY VIDEO

BASIC CONNECTION DIAGRAM





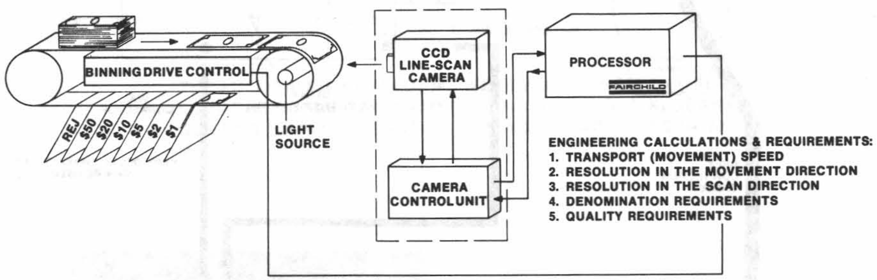
APPLICATION: SCANNING/RECOGNITION SYSTEM

SYSTEM DESCRIPTION

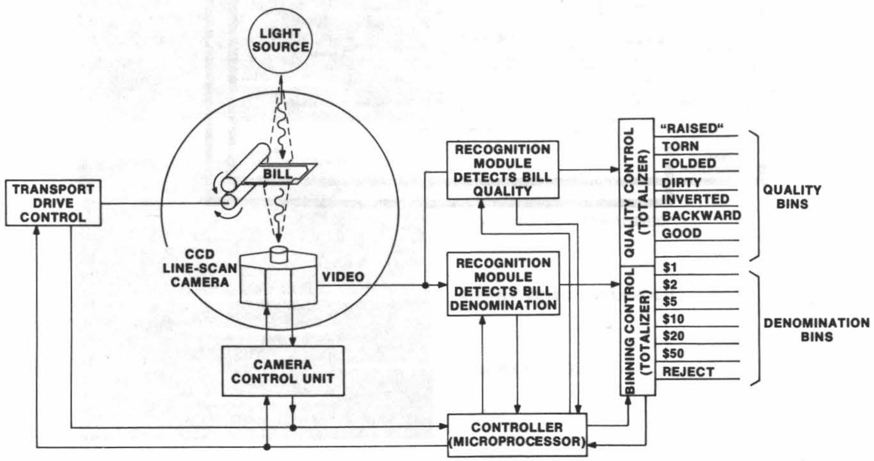
The Line-Scan Camera subsystem is a powerful scanning and/or recognition tool when combined with a computer or microprocessor. The technique used here, shows a rear lighted document being sensed by the line scan camera. A digital representation (ROM) of the desired object is stored in the microprocessor memory and is placed in synchronization with the unknown object located on the transport. When both the camera output and the microprocessor output indicates that a match has been established, the proper binning control is activated to receive the document. If insufficient criteria is available for determination of a match, the binning selection controller places the bill in the rejection bin. When properly programmed, documentation quality as well as value or denomination can be determined.

This technique is adaptable to automatic sorting systems, where only a few (or many) defects must be found in a large population. By implementing object viewing masks in the microprocessor, only certain fields of optical information in the object can be selected for processing. All other areas of the object are ignored.

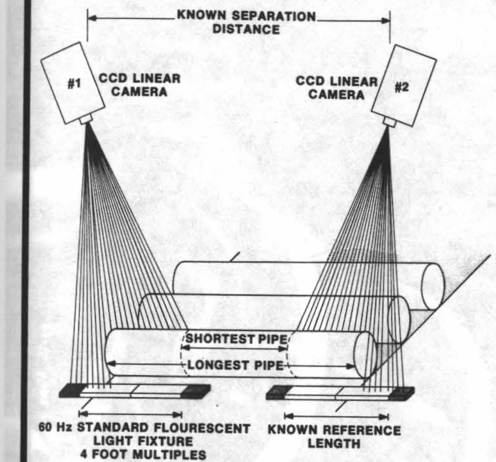
PICTORIAL VIEW SCANNING AND RECOGNITION SYSTEM



BLOCK DIAGRAM SCANNING AND RECOGNITION SYSTEM



PICTORIAL VIEW MEASUREMENT SYSTEM



APPLICATION: MEASUREMENT SYSTEM

FEATURES:

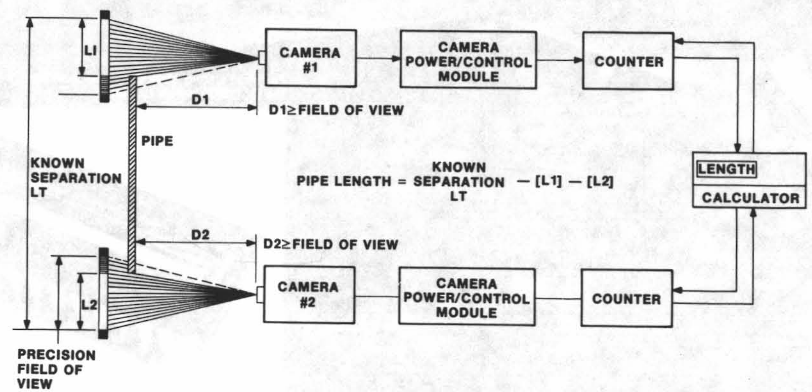
- Standard fluorescent light fixture
- Easy to align and maintain
- Self calibrating feature for
  - length
  - light level (AGC)
- Accurate Calculator permits taking many samples and averaging.

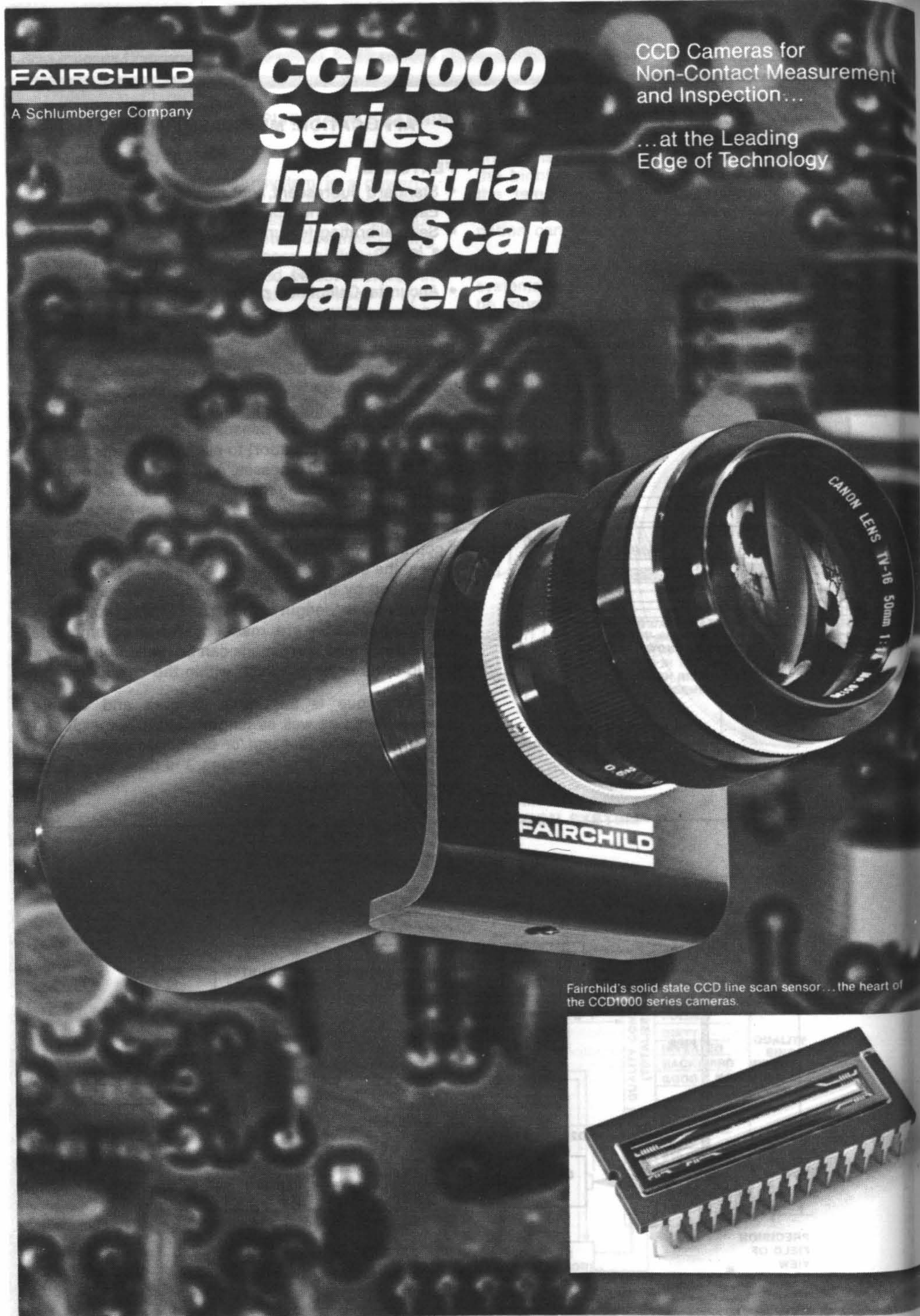
SYSTEM DESCRIPTION

By positioning two CCD Line Scan Cameras outside of the longest object and knowing the separation of the reference end points, length can be determined. The technique utilized here, senses the bottom edge of the object (closest to the floor) to eliminate effects of varying diameters or thicknesses. A standard 60 Hz fluorescent light source facing toward the camera can be used as the illumination source; a good black/white transition is necessary. The output of each camera is fed into a counter with bcd output. Since, the distance (LT) is known, the distance from each edge to the transition is determined by the camera. Subtracting L1 + L2 from LT produces the length of the pipe when corrections for lens magnification are made by the programmable calculator. These corrections can be implemented by a lookup table or an equation within the calculator.

This technique is adaptable to area and volume measurements as well as length. Gap, thickness, and position measurement and/or correction systems can be implemented when the camera is used as a feedback sensor to a controller.

BLOCK DIAGRAM





Fairchild's solid state CCD line scan sensor... the heart of the CCD1000 series cameras.

CCD1000 Series Industrial Line Scan Cameras

- ☐ Charge Coupled Device Image Detectors
- ☐ All solid state
- ☐ Small, compact sealed enclosure
- ☐ Ideal for use in hostile industrial environments
- ☐ Remote operation (up to 200 cable feet)
- ☐ Data rates to 20M pixels per second
- ☐ Line scan rates to 40K lines per second

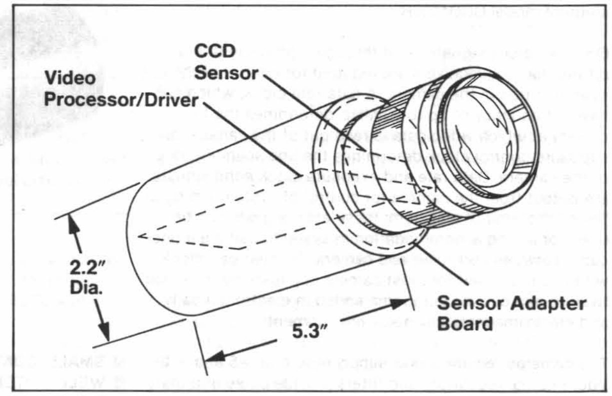
The Fairchild CCD1000 series are small, rugged, solid-state line scan cameras designed for incorporation into non-contact electro-optical measurement and process control systems. System design and implementation using the CCD1000 series cameras are simplified due to the requirement of only two clock input signals to completely control operation of the cameras. The sealed enclosure and remote operation capability make these cameras ideally suited for operation in hostile environments.

The camera can be installed in a water jacket when necessary for environmental protection and located more than 200 feet away from a control unit/power supply.

The cameras are available in resolutions of 512, 1024, or 2048 elements.

Specifications

	CCD1200R	CCD1300R	CCD1500R
Sensor	512 x 1	1024 x 1	2048 x 1
Exposure Time (min)	27μs	52μs	103μs
Line Scan Rate (max)	37K	19K	9.7K lines/sec.
Dynamic Range	>1000:1		
Saturation Exposure	0.67μj/cm² with daylight fluorescent light		
Saturation Signal Voltage	1V P-P, .7V P-P min.		
Spectral Response	400nm-800nm standard		
Video Data Rate (max)	20MHz		
Outputs			
Video	Two time division multiplexed outputs, 1V P-P, 75 ohms		
Clocks	Data rate echo and line sync		
Inputs			
Data Rate Clock Exposure Control Clock	+5 to +20 volts differential		
Power Requirements	+5V @ 500mA max +15V @ 250mA max		
Size (without lens)	Diameter 2.2" (5.7cm) Length 5.3" (13.5cm)		



Industrial Line Scan Cameras
CCD1200R 512-Element
CCD1300R 1024-Element
CCD1500R 2048-Element

CCD Imaging

Description
Fairchild Models CCD1200R, CCD1300R, CCD1500R are rugged line scan cameras designed for incorporation into non-contact electro-optical measurement and process control systems. The model CCD1200R has a resolution of 512 elements per line; the model CCD1300R has a resolution of 1024 elements per line; and the model CCD1500R has a resolution of 2048 elements per line.

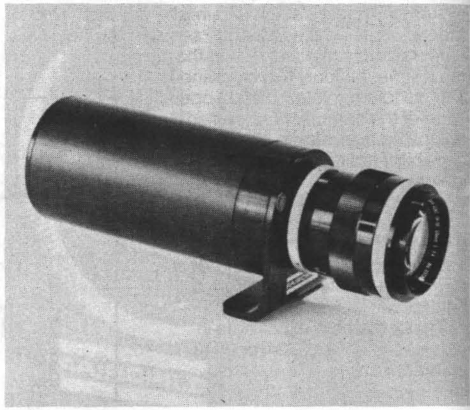
The small sealed enclosure permits the camera to be used in systems where space is limited. The camera can be installed in a water jacket when necessary for environmental protection, and can be located more than 200 cable feet away from a control unit/power supply. A C-mount lens adaptor is standard for the CCD1200R and CCD1300R cameras; a T-mount adaptor is standard with the 2048 element model CCD1500R.

Only two clock signals input through high noise immunity differential line receivers are required for control of the line scan function in the camera. A data rate clock, which can have a frequency of up to 20 MHz, determines the frequency at which video data is read out of the camera: an exposure control clock determines the line scanning rate of the camera. Data rate and exposure clock echo signals are output from the camera for control of system timing at the control unit of a system; these echo signals can be used for timing accommodation in systems using a longer cable between controller and camera. Twisted pair clock wiring can be used for most camera applications; shielded twisted pair cabling is recommended in electrostatically and electromagnetically noisy environments.

The cameras require power supply inputs of +5 and +15 Vdc. Internal regulators and filters provide noise immunity for the bias voltage inputs. Separate force and sense lines allow control of supply voltages and ground potentials at the camera end of long cables.

Two time-division multiplexed analog video outputs are available from coaxial connectors on the camera, at a 75 ohm source impedance. The output video data rate, when measured in pixels per second, is equal to the data rate clock input frequency. Video data is intended to be processed in user-designed circuitry in a control unit as required by the application; simple comparators are sufficient for typical width measurement applications which use black-white binary video while more elaborate analog and/or A-D converted processors are required for systems recognizing gray-scale.

Applications
- NON-CONTACT INDUSTRIAL MEASUREMENT & INSPECTION
- WIDTH/POSITION/DEFECT DETECTION IN PROCESS CONTROL SYSTEMS
- PATTERN RECOGNITION
- CHARACTER RECOGNITION
- IMAGE ANALYSIS FOR COMPUTER CONTROLLED APPLICATIONS



- **SMALL, COMPACT SEALED ENCLOSURE**
- **WELL SUITED FOR USE IN RUGGED INDUSTRIAL ENVIRONMENTS**
- **ALL SOLID STATE**
- **UTILIZES CCD SENSOR: 512, 1024, 2048 RESOLUTIONS AVAILABLE**
- **REMOTE OPERATION (OVER 200 CABLE FT.)**
- **WATER JACKET COMPATIBLE FOR HIGH TEMPERATURE OPERATION**
- **TWO CLOCK INPUTS CONTROL CAMERA**
- **NO GEOMETRIC DISTORTION**
- **1000:1 DYNAMIC RANGE**
- **ELECTRONICALLY VARIABLE DATA RATE AND EXPOSURE TIME**
- **ACCEPTS C-MOUNT OR 35 MM LENSES**
- **VIDEO DATA RATES UP TO 20 MHz**
- **SCAN RATES UP TO 40,000 LINES/SECOND**

Ruggedized Camera Specifications

Camera	CCD1200R	CCD1300R	CCD1500R
Sensor	CCD153 512 × 1 Element Array	CCD133 1024 × 1 Element Array	CCD143 2048 × 1 Element Array
Photo Element Size	13 μm × 13 μm Located on 13 μm centers		
Geometric Distortion	Determined by lens selected		
Dynamic Range	Typically better than 1000:1, excluding clock coupling		
Dark Signal Non-Uniformity (DSNU)	50 mV P-P max. at an integration time of 8.33 ms and T_A = 25°C		
Photoresponse Non-Uniformity (PRNU)	100 mV P-P max. @ 1 V V_{OUT}, measured at T_{INT} = 8.33 ms, T_A = 25°C, using a daylight fluorescent light source		
Saturation Exposure	Typically 0.67 μJ/cm², using a daylight fluorescent lamp light source		
Saturation Signal Voltage	2 V P-P typical, 1 V P-P minimum		
Spectral Response	The camera includes a Corning 1-75 filter		
Video Data Rate	20 M pixels per second maximum (typical)		
Exposure Time (Min)	26 μS	52 μS	103 μS
Scan Rate (Max) Lines/Second	38 K	19 K	9.7 K

Maximum usable exposure time is limited by the dark signal level developed during the integration time. Dark signal level is an exponential function of camera and (consequently sensor) temperature: dark signal level doubles for each 6-8°C rise in temperature. Dark signal level also increases linearly with exposure time.

Functional Description
As is shown by the block diagram, the circuitry within the camera is comprised of logic and driver control of the CCD image sensor, the sensor itself, video buffers and power supply filters. An infra-red reject optical filter and lens mounting adaptor are included in the enclosure.

Image Sensor
The Charge Coupled Device line scan image sensor used in the camera is a monolithic component containing a single row of image sensing elements (photosites or pixels), two analog transport shift registers, and two output sense amplifiers. Light energy falling on the photosites generates electron charge packets which are proportional to the product of exposure time (1 ÷ line scan frequency) and incident light intensity. The photosite charge packets are transferred in parallel to the two analog transport registers in response to an exposure time clock signal input into the camera. The transport registers, in response to the data rate clock, deliver the packets in sequence to an integrated charge sensing amplifier where they are converted into proportional video signal voltage levels.

The model CCD1200R camera uses a selected version of the 512 element Fairchild CCD153 sensor; the model CCD1300R camera uses a selected version of the 1024 element CCD133 sensor; and the model CCD1500R uses a selected version of the 2048 element CCD143 sensor.

The key advantages of Fairchild's isoplanar buried channel CCD sensors for use in the line scan cameras include high data rate capability, high charge transfer efficiencies, low noise, relatively small die sizes, and geometrically precise construction.

Logic and Drivers
Differential line driver input signals are converted into TTL level voltages by the line receivers, and then amplified and shaped for control of the image sensor clock inputs. Single-ended TTL clock inputs can be used if the negative differential input is biased at +1 V; this technique is recommended only for short cable clock inputs and/or relatively slow video data rate operation.

The frequency of the data rate clock input signal determines the rate at which charge packets are transported along the CCD analog shift register. Valid video data from odd-numbered sensor photosites becomes available within 50 ns following a falling edge of a data rate clock signal from camera video output A; the signal from video output connector B becomes valid 50 ns after the rising edge of an input data rate clock.

CCD1200R/1300R/1500R

A positive exposure control input signal causes accumulated photosite data to be transferred within the CCD to the analog transport registers for readout under control of the data rate clock. The interval between exposure control inputs is the sensor exposure time.

As is noted in the timing diagram, the exposure control pulse input width is unimportant for camera operation. The data rate and exposure control inputs need not be synchronized. The only timing restriction is that the interval between exposure control input signals should be greater than the camera resolution (# of elements) times 1/video data rate to prevent addition of old and new charge packet data in the CCD registers.

Video Output Buffers

Sensor video is buffered by two independent unity-gain 75 ohm output impedance buffers to become the camera video outputs. The video signals ride on a dc level of about 4 volts above ground. External processing circuitry can be used to demultiplex the two video signals. The amplitude of each video signal will typically be 1 V P-P at sensor saturation; the video signal waveforms are sampled and held continuous signals with a small high-frequency sampling clock content.

Optical Components

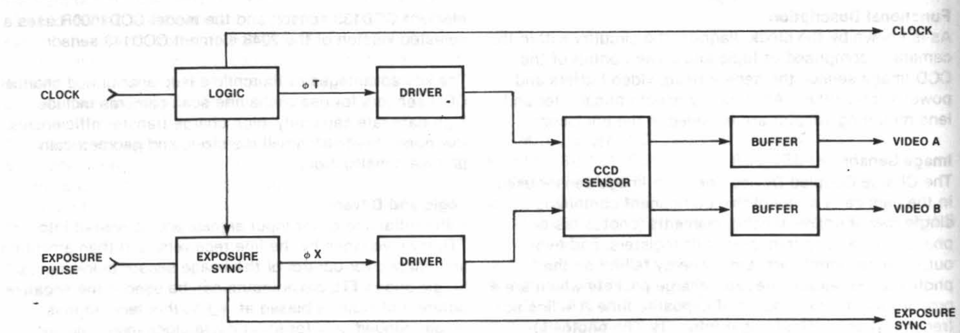
Each photosite in the sensor is 13 microns (0.51 mils) square. Total active array length is 3.3 mm (.131 inches) for the model CCD1200R, 13.3 mm (.52 inches) for the model CCD1300R, and 26.6 mm (1.04 inches) for the model CCD1500R.

The 512 and 1024 element array lengths are compatible with C-mount lens. The 2048 element array should be used with a 35 mm film camera format lens. Various focal length lenses can be provided by Fairchild as camera accessories.

When ordering, specify device type LENS25C for 25 mm; LENS50C for 50 mm, standard C-mount lens.

A Corning type 1-75 infra-red absorption filter is made a part of the standard cameras. The filter transmission convolved with the spectral responsivity of a silicon CCD sensor gives the camera a response ranging from about 400 to 800 nm, with a peak response at about 700 nm.

Block Diagram



CCD1200R/1300R/1500R

Camera Connections

J1

Name	Pin
MC1⁺	6
MC1⁻	13
XTO⁺	5
XTO⁻	12
MC2⁺	8
MC2⁻	15
XT2⁺	7
XT2⁻	14
+5 FORCE	4
+5 SENSE	11
+15 FORCE	2
+15 SENSE	9
GND FORCE	3
GND SENSE	10
GND SHIELD	1

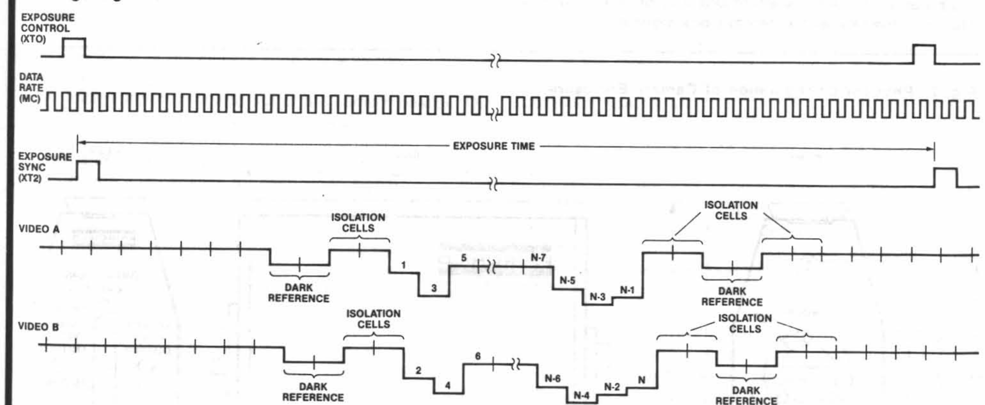
J3	J4
VIDEO A	VIDEO B

Inputs:
- Data Rate Clock (MC1), 20 MHz MAX, Differentially Received
- Exposure Control Clock Pulse (XTO), 25ns Min. Width, Differentially Received
- +5 V @ 500 mA MAX
- +15 V @ 250 mA MAX
- Ground

Outputs:
- Data Rate Clock (MC2), Differentially Driven
- Exposure Sync (XT2), Differentially Driven
- Video A, 75 Ohm Source Impedance
- Video B, 75 Ohm Source Impedance
- +5 V Sense
- +15 V Sense
- Ground Sense

Dimensions:
- Diameter 2.25″
- Length 5.125″ Without Lens

Timing Diagram



Notes

N = Number of elements in the array, i.e., 512, 1024, or 2048

XTO = At least 25 ns width, may be asynchronous and should not occur while video data is being clocked out

MC = 20 MHz MAX. Data rate out equals data rate in plus 50 ns (typical camera propagation time) and any transmission line delay

XT2 = Time interval between leading edges determines integration time

Ordering Information

When ordering, specify device type

CCD1200R	CCD1300R	CCD1500R
512 x 1 Element Array	1024 x 1 Element Array	2048 x 1 Element Array

For further information please call your nearest Fairchild Sales Office. For technical or applications assistance call (415) 493-8001.

FAIRCHILD
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CCD

CCD2000C • CCD2100C

Area Camera Subsystems

Description
The CCD2000C and CCD2100C area camera subsystems utilize Fairchild's CCD221 and CCD211 area image sensors respectively. They are intended for use in various scientific and industrial electro-optical instrumentation systems which can take advantage of the precise geometric accuracy, wide dynamic range and wide spectral response of the monolithic CCD silicon detectors.

The CCD221 sensor is organized as a matrix of 488 x 380 elements providing the CCD2000C with full NTSC black and white television resolution when operated at a 30 Hz frame rate (7.16 MHz video data rate). The negative-sync 1 V_{pk-pk} composite video signal output of the CCD2000 is delivered in 2-field per frame line-interlaced form. The camera subsystem may be operated at up to 60 frames per second when driven by an external clock signal.

The CCD211 sensor is organized as matrix of 244 x 190 elements providing the CCD2100C with full NTSC black and white television resolution over the center 25% area of a TV display monitor. Structurally similar to the CCD2000C, the CCD2100C will operate at a frame rate of 120 Hz at a 7.16 MHz data rate and may be operated to a 240 Hz frame rate with external clock signals.

Fig. 1 Camera Block Diagram

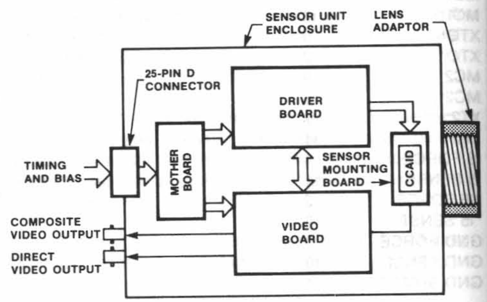
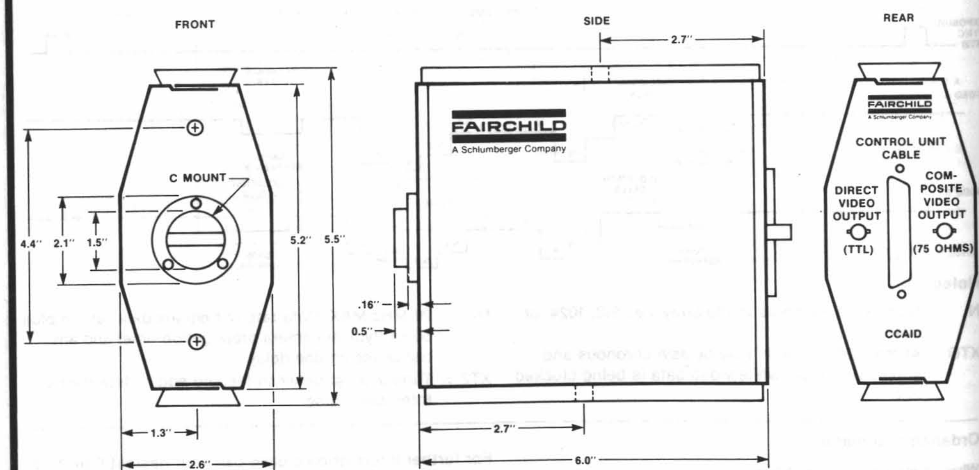


Fig. 2 Physical Configuration of Camera Enclosure



Functional Description Subsystem

The standard CCD2000C and CCD2100C area camera subsystems consist of a system control unit, a 5-foot interconnecting cable and a camera enclosure.

Camera
The camera consists of four printed circuit boards *(Figure 1)* contained in a metal enclosure *(Figure 2)*. The boards are a driver board, a video processor board, a sensor mounting board, and a rear panel mother board. The enclosure *(Figure 2)* provides dovetail-slides at the top and bottom which can be used for optical bench installations, a 1/4"-20 tapped hole in the bottom dovetail which can be used for tripod camera mounting, and two 8-32 tapped holes in the camera front panel which can be used for faceplating mounting. Faceplate mounting is recommended for fixed installations where vibration-free operation is necessary.

The camera enclosure includes a lens adaptor which has a female 1"-32 thread for use with a C-mount lens. A Corning type 1-75 infra-red reject filter is included in the optical path for shaping of the spectral responsivity curve of the CCD image detector.

The rear panel of the camera supports a 25-pin D connector which provides connections for digital and bias voltage inputs into and out of the camera boards. The rear panel also contains two female BNC connectors which provide, respectively, composite processed video output and buffered video direct from the sensor. The output source impedance for each video signal is 75 ohms.

Composite video is processed on the video board to include a negative composite sync signal which is at standard U.S. television rates when the internal crystal controlled clock oscillator on the timing logic board is being used. This 14.32 MHz oscillator provides a video readout rate of 7.16 Megapixels per second, a scanning line frequency of 15.73 kHz, a field rate of 60 Hz, and a frame frequency of 30 Hz. Output data is in a two-field-per-frame, fully interlaced format. There are 525 lines in each frame, including the vertical blanking interval. Pixel rates, line rates, field rates, and frame rates are all multiplied by the ratio of the selected external clock frequency to 14.32 MHz when an external video clock input is used as the master clock in the timing logic board.

The sync signal amplitude at the sensor unit composite video output is 0.7 V_{pk-pk} into 75 ohms. Video black is 0 ± 0.1 V. An internal gain control allows video white to be set to 0.7 V at sensor saturation. An AGC amplifier with 20 dB dynamic range can be incorporated into the composite video processor by connecting together two pins on the D connector. This function is performed by the AGC select switch on the control unit. The video output is linear with the product of image brightness and sensor exposure time; i.e., the sensor unit has a gamma of 1.0.

Access to the unprocessed video signal direct from the sensor is provided to permit use of special signal processing circuitry external to the sensor unit. This video output, which may be terminated by 75 ohms, is buffered by an emitter follower only. The direct signal rides on a dc voltage which will be from 6-10 V above ground. The direct signal amplitude at sensor saturation will be between 0.2 and 1.5 V_{pk-pk}. The sampled-and-held direct signal output contains a sampling clock pulse, about 30 ns in duration at the video data rate, which can be removed with a low-pass filter.

The binary video output of the sensor unit is provided by a precision comparator. One side of the comparator is driven by the video processor signal at the output of the optionally-used AGC stage, the other comparator input is the threshold voltage applied to a pin of the D connector (controlled by a potentiometer in the subsystem control unit).

Timing signal inputs to the sensor unit are balanced differential digital waveforms supplied to the driver board through the rear panel D connector. These signals are ordinarily provided by a timing logic card in the subsystem control unit. Their generation is controlled by the internal or external master clock for this board. The line receivers used are Fairchild type 9613, the line drivers are Fairchild type 9612.

The simple logic of the driver board converts a square wave master clock input into the complimentary clock signal required for horizontal transport of data in the CCD sensor, and generates the sample-and-hold clock needed by the CCD output circuit. The frequency of the horizontal clock applied to the CCD, and hence the sensor video data rate, is 1/2 the frequency of the input clock square wave.

Vertical transport, and field transfers of data from photosites to CCD vertical registers, are controlled by ϕV and ϕP driver board input signals. Sync and blanking signals are buffered on the driver board and then delivered to the video processor.

Control Unit

The control unit for the CCD2000C/CCD2100C camera subsystem is a 10 by 8-1/2 by 5 inch metallic enclosure which is designed for bench-top installation *(Figure 3)*. The control unit provides operating bias voltages and timing signals to the camera, provides access connectors for the digital (TTL level) input and output signals of the subsystem, and contains the few operating function controls for the subsystem.

The control unit power input is fuse protected. Line voltages of 115 or 230 Vac ± 10%, 50 - 400 Hz may be used.

The principal circuitry within the control unit is contained on a single printed circuit board designed as a "timing logic card". The TTL hardware logic on this card includes horizontal and vertical counter chains which drive PROMs programmed for generation of CCD sensor and TV-sync timing signals. The counter chains, which can be driven by either an internal crystal-controlled master oscillator or an external TTL-level master clock input signal, also develop numerical-sequence binary-coded address data which identifies individual pixel outputs from the sensor in the camera.

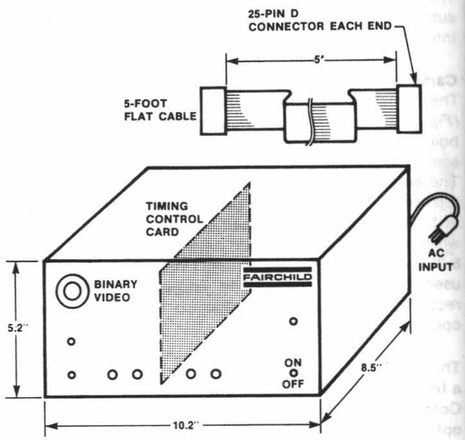
The control unit contains two card slots which are pre-wired to accept the optional pixel-address buffer card and the sweep generator card described below. These cards will be installed in the control unit if ordered with a CCD2000C or CCD2100C camera subsystem.

The control unit panels support BNC connectors which provide user access to the following system TTL output signals: Binary Video, Composite Blanking, Field (Odd) Sync, Composite Sync, Video (Data Rate) Clock, Exposure Sync, Vertical Sweep and Horizontal Sweep. The control unit will accept, through BNC connectors, TTL waveforms for external Exposure Control and external Video Data Rate clock inputs. Panel mounted controls are Power Off/On, AGC Off/On, the Video Clock Internal/External select switch, and a potentiometer for adjustment of the Binary Video threshold voltage. A 25-pin D connector provides I/O connection to the camera cable and a 50-pin D connector provides user access for digital I/O signals.

Cables

The CCD2000C and CCD2100C subsystems include a flat cable five feet in length for interconnection of the control unit and the camera. The cable carries timing signals as balanced differential clock waveforms, and bias voltages as required. High noise-immunity line drivers and receivers are used in the control unit and

Fig. 3 Control Unit



the camera; the subsystems have been successfully operated in electro-magnetically noisy environments with cable lengths greater than 100 feet.

Subsystem Options

The CCD2000C and CCD2100C camera subsystems can be ordered with the options described below for flexibility.

Remote Sensor Mounting Kit (REMOKIT)

REMOKIT is a kit of components which permits the sensor to be mounted remote from the sensor unit enclosure. It is intended for use in those applications where the sensor will be installed in a special optical fixture or cooled chamber and, hence, needs to be physically separate from the sensor enclosure containing the video processing and CCD drive boards.

REMOKIT contains a pre-assembled plug-in replacement for the sensor unit front panel, a sensor mounting board, a board with a set of connectors to interface the sensor mounting board with the modified sensor unit front panel, a 9" terminated cable and a BNC connector. The 9" cable can be used with a CCD221 or CCD211 sensor operating at standard TV scanning rates with minimal loss of performance. Longer cables can be used at slower sensor scan rates.

The sensor mounting board is approximately 1" x 2". The two remote sensor adaptor boards are about 3.6" x 1.5". Each end of the sensor cable is terminated by a 25-pin male D connector. The video cable ends are terminated by male BNC connectors.

Address Buffer Card (ADDBUFF)

ADDBUFF is an address buffer card that buffers the pixel and line address signals from the timing logic card and makes them available in 18 parallel-by-bit binary coded TTL. The address buffer card is designed to fit into a pre-wired slot in the control unit. The binary coded output appears at a 50-pin D connector on the control unit rear panel.

Sweep Waveform Generator Board (SWEEP)

SWEEP is a sweep waveform generator board which uses two digital-to-analog converters to generate vertical and horizontal ramp sweep waveforms which can be used to drive the scan electronics of CRT displays on certain types of hard-copy printers.

The input to the d/a converters are the binary coded pixel and line address outputs of the timing logic card. Sweep waveform timing automatically tracks data rate and exposure time clocks, since it is digitally generated. The amplitude of the ramp signal output is 1 V_{pk-pk}.

SWEEP is designed for installation in a pre-wired slot in the control unit.

FAIRCHILD
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CCD

PIXEL LOCATOR

GENERAL DESCRIPTION

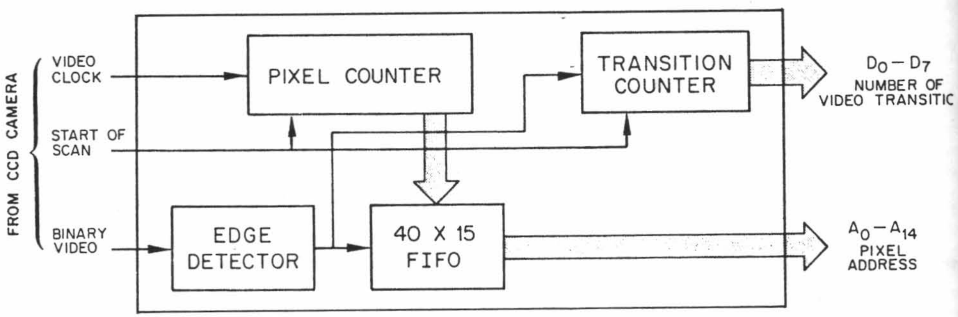
The Pixel Locator is an optional accessory which can be ordered for use with any of the Fairchild standard-product Line Scan Camera Subsystems; the 256-element CCD1100, the 1024-element CCD1300 or the 1728-element CCD1400.

The accessory is a single printed circuit board which is installed in a 3" X 6" X 10" enclosure designed as a companion to the control unit with the standard subsystem family. All required bias voltage and camera signal input connections are made by a single 15-wire cable which is provided for interconnection between the Pixel Locator and control unit. A mating 50-pin connector is provided to allow user construction of a cable for accessing of the Pixel Locator I/O ports.

The primary electrical function of the Pixel Locator is generation of a set of digital output data words which indicate the pixel address locations where white-to-black and black-to-white transitions occur in the Binary Video signal from the associated Line Scan Camera. A pixel is a "picture element", which physically corresponds to a discrete photosite in the monolithic Charge Coupled Device image sensor employed for optical detection in the camera. There are 256 pixels (and hence 256 corresponding pixel addresses) in the CCD1110 camera, 1024 pixels in the CCD1310, and 1728 pixels in the CCD1410.

First-In First-Out buffer memory storage is provided for the set of address words detected by the Pixel Locator, which allows the users system to access address data at any rate up to 2M words per sec. The sequentially-available set of digital address output words permits many non-contact measurement application problems to be resolved with simple binary subtraction or digital display circuitry.

As a secondary function, the Pixel Locator also provides an 8-bit output word which indicates the number of video signal transitions which were detected in a preceeding camera line scan readout.



PIXEL LOCATOR BLOCK DIAGRAM

ORDER INFORMATION

To order the Pixel Locator option, specify the following:

For the CCD1100 camera system order CCD1120-02

For the CCD1300 camera system order CCD1320-02

For the CCD1400 camera system order CCD1420-02

Complete documentation is included in the shipment of the accessory. This includes more detailed description of the operation of the module, schematic diagrams and interconnection diagrams between the Camera Control box and Pixel Locator box.

The pixel locator accessory is capable of performing other specialized functions as well as providing other outputs which can be useful for various types of applications. For further details, please consult the factory at 415-493-8001.

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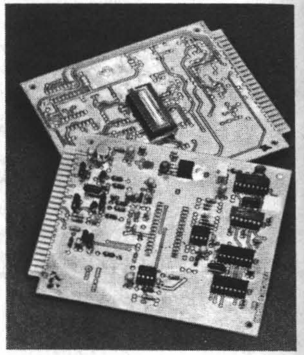
CCD

Design Aids for CCD Line Scan Imaging Sensors

Fairchild offers a series of printed circuit boards for use as construction aids for experimental systems using CCD line scan image sensors. These design development boards are fully assembled and tested, and require only power supplies and an oscilloscope to display the video information corresponding to the image positioned in front of the sensor.

A typical board (block diagram) includes an on-board variable-frequency clock generator that can be overridden by an external input, logic circuitry for timing drive signals, drivers to interface the TTL logic to CCD levels, a socket for mounting the device on the board, video buffer circuits and simple video processing electronics. Design development boards are available for all CCD line scan image sensors.

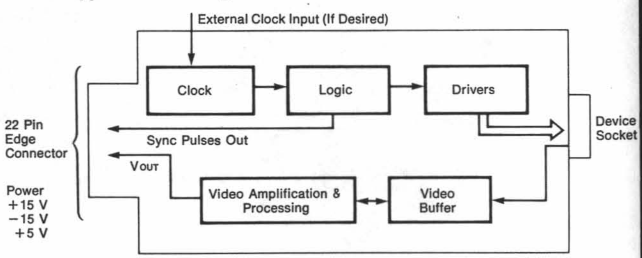


Ordering Codes

Design Aid Ordering Code	For Use With	
CCD111DB	CCD111DC	256x1 Element Line Scan Sensor
CCD133DB	CCD133DC	1024x1 Element Line Scan Sensor
CCD121HB	CCD121HC	1728x1 Element Line Scan Sensor
CCD122DB	CCD122DC	1728x1 Element Line Scan Sensor
CCD142DB	CCD142DC	2048x1 Element Line Scan Sensor
CCD143DB	CCD143DC	2048x1 Element Line Scan Sensor

To operate the board, supply +5 V, +15 V and −15 V through a 22-pin standard edge connector to the PC board. Video information, typically 1 V peak-to-peak, as well as synchronization pulses are supplied to the connector for display on an oscilloscope.

Typical Block Diagram for a CCD Printed Circuit Board



LID II DEMONSTRATION BOARD

The LID II demonstration board, FAIRCHILD Drawing No. 710490 is constructed on a standard size PC card 4-1/2 by 5 inches. The PC board is wired to interface with a 44 position double readout connector with 0.158 inch ℄-℄ finger spacing (TRW/CINCH 251-22-30-160 or equivalent). An external power supply providing 15V at 200ma to fingers 1 and A is required. Other board connections are given on Schematic 710492.

The demonstration board is intended for use as an aid in understanding operation of the LID II devices and for construction of experimental systems using the 1728 element CCD122 or the 2048 element CCD 142 charge coupled linear image sensing device. The preassembled board provides all the bias voltages and clock waveforms required for typical operation of the LID II image sensors, plus an elementary processor circuit providing a low impedance video output signal.

The CCD sensor is mounted on the back side of the circuit board. The user can easily mount a lens in front of the sensor to complete a fully functional linear image sensing system, with no experimentation or breadboard costs.

The LID II demonstration board includes a VCO (U1) which controls the video data rate from .5 to 2MHz, and a one-shot (U7) which controls exposure time between ϕ_T pulses. Both the master clock and exposure one-shot may be removed from the board and external signals injected at connector fingers 5 & 3 to control board operation. The master clock operates at twice the video data rate and four times ϕ_T, transport clock frequency. Flip-flop U2A and U2B divide the clock frequency by four. This lower frequency signal is applied to the ϕ_T driver (1/2 of U4), a FAIRCHILD 9644 dual TTL to MOS driver.

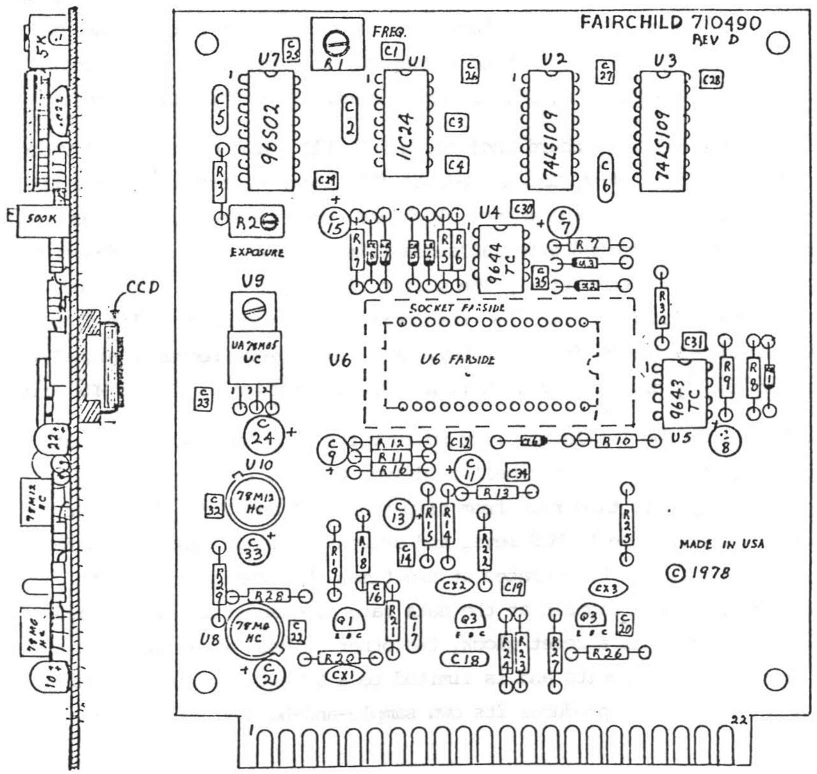
Driver U4 shifts the TTL level clock to 10 volts and clocks the ϕ_T input of image sensor U6. The other half of driver U4 gets its single input pulse at the exposure time rate from flip-flops U3A and U3B. ϕ_X driver converts this TTL pulse to MOS level and drives the image sensor transfer gate ϕ_X of U6. Driver U5 operates at two times the frequency of ϕ_T to provide two different signals at the data rate frequency; one is applied to the image sensor as a reset clock, the other is used as a data rate clock for external circuits and is limited to a 5V swing by zener diode CR1. The image sensor produces its own sample-and-hold clock on chip.

The amplitude of the internal sample pulse is controlled by zener diode CR2 in series with diode CR3 to ground which forms a pulse amplitude clipping network for the $\emptyset_S$ pulse.

The end of scan pulse (VEOS) is buffered by Q3 and sent off the board at connector finger 13 through 75 ohm resistor R27. This pulse indicates that the readout of a line of video information is completed. The EOS pulse was injected into the EOS register by transfer pulse $\emptyset_X$ applied to the sensor U6 at pin 16.

The video output register signal (V_{OUT}) passes through a simple 2MHz cutoff low pass filter formed by Q1, Q2 and associated capacitance and resistance circuits and is then routed off the board at connector finger 11 through 75 ohm resistor R24. Capacitors CX1, CX2 and CX3 may be installed by the user to provide high frequency rolloff as required to reduce high frequency on the output video signal.

SIDE VIEW FRONT VIEW



CCD133DB AND CCD134DB DESIGN DEVELOPMENT BOARDS

The Fairchild CCD133DB and CCD143DB design development boards are printed circuit cards which are intended for use as educational aids for gaining understanding of the operating characteristics of Fairchild CCD133 and CCD143 line scan image sensors and for use in assembly of experimental systems using the line scan sensors. The design development boards are sold fully assembled and tested, and require only connection of a single power supply input of +20V and connection of an oscilloscope to display the video information detected by the sensor.

The boards, Figure 1, are 4 1/2 by 5 inches. A socket for installation of the charge coupled device line scan sensor is mounted centrally on the back (wiring) side of the card. The user can readily mount a lens in front of the sensor if required for his study. Board I/O connections are made through a 44 position double readout edge card connector with .156 inch center-to-center finger spacings. The edge connector is compatible with a TRW/CINCH type 50-44B-10 or equivalent.

When a CCD143 is being used with a design development board, it should be installed in the sensor connector in normal fashion. When a CCD133 is being used, it should be inserted into the center of the socket so that socket terminals 1, 14, 15, and 28 are left open.

The board circuit, Figure 2, requires a power supply positive input of 20±2V at 300mA maximum to Pins 1 and A of the edge card connector. The negative power supply line should be wired to the principle board ground contact on edge Fingers 22 and Z.

Three regulators on the design development boards provide a V_{DD} sensor supply voltage which is adjusted to +15.0V, a clock high level voltage which is set to +12.0V, and a +5V V_{CC} required by the TTL logic circuitry.

For normal self-contained operation of the board, Connector Terminal 17 is left open. Voltage Controlled Oscillator U1 generates a video clock signal which may be adjusted from approximately 5 to 20 MHz by potentiometer R1. The frequency of the video clock square wave from U1 is divided by two by flip-flop U2A; one-half of MOS driver U4 amplifies the flip-flop output to provide the ϕ_T transport clock signal required by the CCD image sensor. The normal amplitude of the ϕ_T clock signal at the sensor terminal is from a low of about 0.5V to a high of about 11.5V, in accordance with the sensor data sheet recommendations. Sensor characteristics at other clock conditions can be evaluated by adjustment of R28.

One-shot U7A and JK flip-flop U2B develop a properly synchronized ϕ_X signal which is amplified by the second half of the 9644 driver U4. The interval between ϕ_X pulses is the exposure time for the sensor; exposure time may be adjusted by R2.

In keeping with good high frequency engineering practice, damping resistors R6 and R7 are used in the MOS driver output lines to minimize overshoot and ringing contents in the clock signals supplied to the CCD. Clamp diodes CR3 and CR4 are used to prevent CCD clock signal excursions below ground; negative clock line transients at the CCD terminals can cause charge-injection which may result in an apparent increase in the dark signal non-uniformity of the sensor.

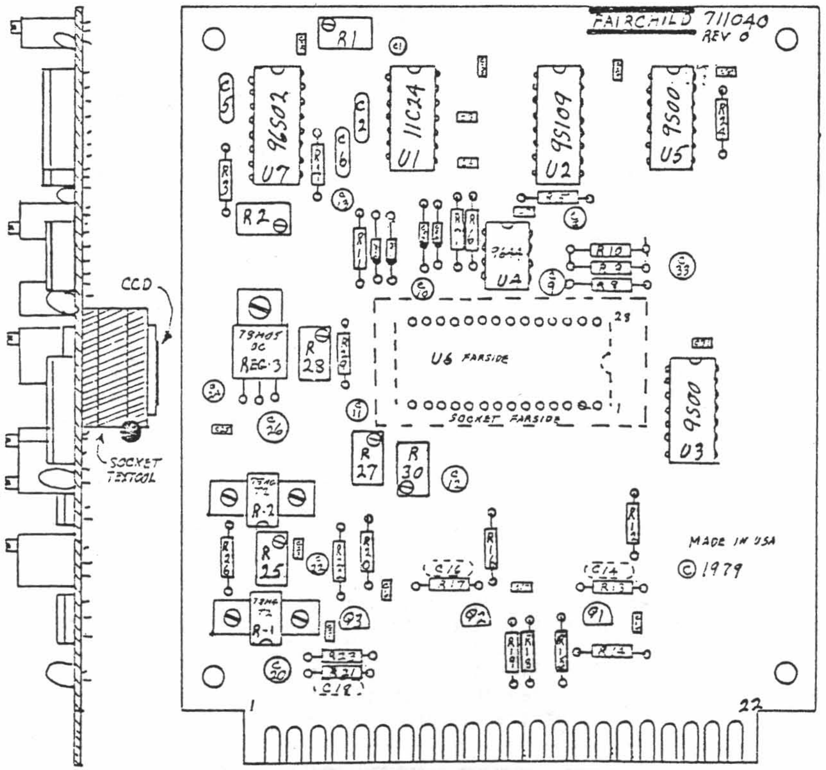
If Finger 17 of the card is held low, the ϕ_T driver will respond to an external data rate clock input on Pin 5 and an external exposure control input to Pin 3. The combined video data rate for the sensor will be equal to the frequency of the clock signal supplied to Pin 5. Sensor exposure intervals are terminated by low-to-high transition on Pin 3.

Connector Figures 7 and 9 provide exposure time and data rate clock output signals for external usage; i.e., for synchronizing an oscilloscope for display of the sensor output signals.

The dc bias voltage applied to the V_T transport register electrodes of the CCD is controlled by R30. This voltage is typically 0.55 times the clock high voltage being supplied to the sensor for best performance. Bias voltage V_{EI} can be set to about 10.5V by R27 to obtain the white reference element output with the video data stream, or it can be increased to V_{DD} to disable the white reference level generating circuitry within the sensor.

The video signals at the two output ports of the CCD line scan sensor are buffered by emitter followers Q2 and Q3 and then made available on connector Fingers 11 and 15. If long co-axial cables are wired to the outputs, the cables should be terminated in 75 ohms for best frequency response. The cable terminations will reduce the video signal amplitude by one-half.

The sensors end-of-scan output is also buffered by an emitter follower and is then made available on Pin 13. This signal can be amplified and clipped for use as a system synchronizing pulse if desired.



FAIRCHILD
A Schlumberger Company

CCD

Signal Processing Products

The capability to manipulate information in the form of discrete charge packets makes CCD technology ideal for analog signal processing.

Fairchild signal processing components are monolithic silicon structures comprised of CCD analog shift registers, charge injection ports, and output charge-sensing amplifiers. They can be advantageously used for delay and temporary storage of analog video signals. The time delay for data transit through the CCD register is precisely controlled by the frequency of the externally supplied transport clock signal. Fairchild signal processing components include a sample-and-hold signal output stage for ease of application.

Fairchild video delay modules are printed circuit board structures which include the CCD321A2 device and are sold as fully assembled and calibrated units. The module is equipped for use as a variable delay circuit, using either an externally supplied or internal variable frequency clock, or for temporary analog data storage in a stopped-clock mode.

Typical applications for the CCD signal processing components and modules include time base correction for video tape recorders, fast input-slow output data expansion systems for A-D converter systems, comb filter realizations, drop-out compensators, and other analog applications up to frequencies of 30 MHz data rate.

CCD321A Variable Analog Delay Line 455/910 Bit

Th CCD321A is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321A consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

The CCD321A can be used in applications ranging from video fre- frequencies to audio frequencies. A complete TV line of 63.5 μs can be stored with a sampling frequency of 14.318 MHz (four times color subcarrier frequency of 3.58 MHz). Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321A also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.

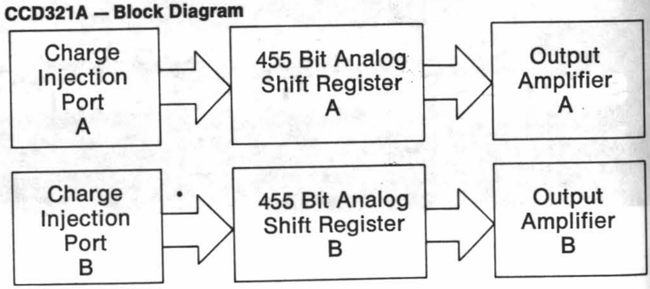
The CCD321A is available in four different classes as follows:

Device	Application
CCD321A-1	Broadcast quality video delay line
CCD321A-2	Industrial video delay line
CCD321A-3	Time base compression and expansion delay line
CCD321A-4	Audio delay line

CCD321A Features

- Electrically variable analog delay line for audio and video applications.
- 1 H video delay line capability with broadcast quality performance.
- Excellent bandwidth at video and audio rates due to buried channel technology.
- Wide range of data rate: From 10 kHz to 20 MHz per 455 section.
- High signal to noise ratio — Video: 58 dB, Audio: 65 dB.

CCD321A — Block Diagram



CCD323A Video Delay Line With On-Chip Drivers 283 ½-Bit

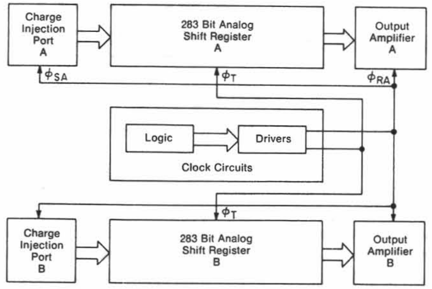
The CCD323A is a 283 ½-bit, dual channel, high speed video delay line with on-chip clock drivers and logic circuits greatly simplifying external circuit design. Only one TTL level clock is required by the user to operate the device, thereby saving many external components as well as board space.

With 283 ½-bits length and clocking done at ≅4.4 MHz, the device produces a delay of ≅64 μsec. to ideally suit PAL TV applications. However, the device is useful in many high speed applications using a delay line shorter than the CCD321A.

CCD323A Features

- Electrically variable analog delay line.
- 64 μsec. at 4.4 MHz clock rate (PAL TV).
- On-chip clock circuits. Requires one external clock. Simplifies external circuit design.
- Excellent bandwidth at video data rates due to buried channel technology.
- Wide range of data rates: From 10 kHz to 15 MHz.
- High signal to noise ratio.

CCD323A — Block Diagram



CCD321M Video Delay Module

The CCD321M is a complete delay module intended for use in video signal processing systems where precisely controlled delay or temporary storage of analog information is required. The module is a printed circuit board containing a Fairchild CCD321 dual 455-bit analog shift register, input and output signal processing circuitry, and the required clocking signal sources and bias voltage controls. The module requires a single +20 V power supply input for operation.

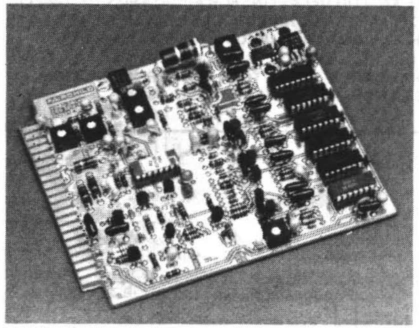
The delay time of analog signals through the CCD321M is precisely controlled by the clock signal frequency which can be provided by an external source or obtained from an internal VCO. The CCD321M can be used as a 910-bit one horizontal line (1 H) delay for TV video bandwidths of 5 MHz when operating with a 4 × 3.58 = 14.3 MHz clock frequency, serve as a temporary analog store for a full-bandwidth TV line, or can be used as an adjustable delay by controlling either the internally generated or external input clock.

The CCD321M can also be used as two 455-bit registers for delay of two independent analog signals.

Typical video applications for the CCD321M include time-base correctors, video re-synchronizing systems, comb filter realizations, moving target indicators and signal-to-noise enhancement systems. Other applications include time-base compression and expansion systems, phase delay equalizers and general purpose analog delay.

CCD321M Features

- 1 H delay line performance
- Electrically variable delay
- Adjustable delay—by clock control
- Wide signal bandwidth — 5 MHz
- High S/N ratio — 55 dB
- Dual 455-bit or single 910-bit delay
- No drift — delay dependent on clock frequency
- Internal or external clocking
- Temporary storage operation controlled by a single TTL input line
- Single polarity power supply — +20 V



CCD321A

455/910-BIT ANALOG SHIFT REGISTER

CHARGE COUPLED DEVICE

GENERAL DESCRIPTION—The CCD321A is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321A consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

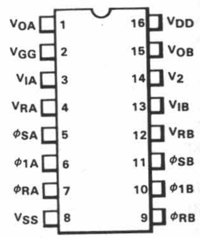
The CCD321A can be used in applications ranging from video frequencies all the way down to audio frequencies. A complete TV line of 63.5 μs can be stored with a four times color subcarrier sampling frequency of 14.318 MHz. Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321A also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.

The CCD321A is an improved pin-for-pin replacement for the CCD321. The CCD321A comes in four different classes as follows:

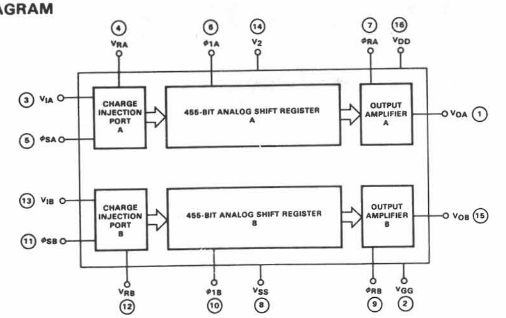
DEVICE		APPLICATION
CCD321A-1		Broadcast quality video delay line
CCD321A-2	±40-25	High quality video delay line
CCD321A-3		Time base compression and expansion delay line
CCD321A-4	± 13-38	Audio delay line

- ELECTRICALLY VARIABLE ANALOG DELAY LINE FOR AUDIO AND VIDEO APPLICATIONS
- 1 H VIDEO DELAY LINE CAPABILITY WITH BROADCAST QUALITY PERFORMANCE.
- EXCELLENT BANDWIDTH AT VIDEO AND AUDIO RATES DUE TO BURIED CHANNEL TECHNOLOGY.
- WIDE RANGE OF DATA RATE: FROM 10 MHz TO 20 MHz PER 455 SECTION.
- HIGH SIGNAL TO NOISE RATION—VIDEO: 58 db, AUDIO: 65 db.

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

ϕ_{1A}, ϕ_{1B}	Analog Shift Register Transport Clocks
ϕ_{SA}, ϕ_{SB}	Input Sampling Clocks
ϕ_{RA}, ϕ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA}, V_{IB}	Analog Inputs
V_{RA}, V_{RB}	Analog Reference Inputs
V_{OA}, V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

FUNCTIONAL DESCRIPTION — The CCD321A consists of the following functional elements illustrated in the Block Diagram:

Two Charge Injection Ports — The analog information in voltage form is applied to two input ports at V_{IA} (or V_{IB}). Upon the activation of the analog sample clocks ϕ_{SA} (or ϕ_{SB}) a charge packet linearly dependent on the voltage difference between V_{IA} and V_{RA} (or V_{IB} and V_{RB}) is injected into analog shift register A (or B).

Two 455-Bit Analog Shift Registers — Each register transports the charge packets from the charge injection port to its corresponding output amplifier. Both registers are operated in the 1-1/2 phase mode where one phase (ϕ_{1A} or ϕ_{1B}) is a clock and the other phase (V_2) is an intermediate dc potential. Phases ϕ_{1A} and ϕ_{1B} are completely independent. V_2 is a dc voltage common to both registers.

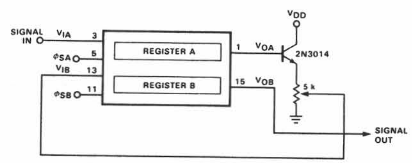
Two Output Amplifiers – Charge packets from each analog shift register are delivered to their corresponding output amplifier as shown in the circuit diagram. Each output amplifier consits of three source follower stages with constant current source bias. A sample and hold transistor is located between the second and third stage of the amplifier. When the gate of the sample and hold transistor is clocked (ϕ_{RA} or ϕ_{RB}) a continuous output waveform is obtained as shown in the timing diagrams. The sample and hold transistor can be defeated by connecting ϕ_{RA} and/or ϕ_{RB} to V_{DD}. In this case the output is a pulse modulated waveform as shown in the timing diagram.

MODES OF OPERATION — The CCD321A can be operated in four different modes:

455-Bit Analog Delay — Either 455-bit analog shift register can be operated independently as a 455-bit delay line. The driving waveforms to operate shift register A is shown in Fig. 10. The input voltage signal is applied directly to V_{IA}. The input sampling clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of register A. The input voltage A_1 which is sampled between $t = 0$ and $t = t_c$ appears at the output terminal V_{OA} @ $t = 910t_c$. If the sample and hold circuit is not used then the output appears as a pulse amplitude modulated waveform as shown in the diagram. In that case ϕ_{RA} (pin 7) should be connected to V_{DD} (pin 16). If the sample and hold circuit is used than the output appears as a continuous waveform. Here ϕ_{RA} (pin 7) should be clocked coincident with ϕ_{SA} (pin 5) and the two pins can be connected together.

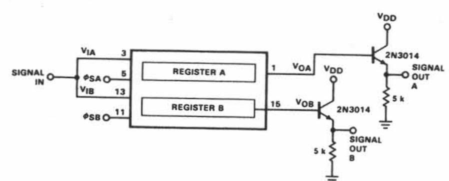
Analog shift register B can be operated in an analogous manner with V_{IB} as the analog input, ϕ_{1B} as the transport clock, ϕ_{SB} as the input sampling clock and ϕ_{RB} as the output sample and hold clock.

910-Bit Analog Delay in Series Mode — The two analog shift registers A and B can be connected in series to provide 910 bits of analog delay as shown in the schematic below. The analog signal input voltage is applied to V_{IA}. The output of register A is connected to the input of register B with a simple emitter follower buffer stage. In order to insure proper charge injection of register B, V_{RB} should be adjusted. The timing diagram shown in Fig. 10 applies in this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{SA} = \phi_{SB}$, $\phi_{RA} = V_{DD}$, and ϕ_{RB} is clocked.



910-Bit Analog Delay in Multiplexed Mode — The two analog shift registers can be connected in parallel to provide 910-bit of analog delay as shown in the schematic below. The analog signal input voltage is applied to both V_{IA} and V_{IB}. The outputs at V_{OA} and V_{OB} can be combined as shown in Fig. 8 to recover the analog input information.

The necessary waveforms to operate the device in this mode is shown in Fig. 11. In this case ϕ_{SA} samples the analog input A_1 at V_{IA} between $t = 0$ and $t = t_c$. ϕ_{SB} samples the analog input B, at V_{IB}, between $t = t_c$ and $t = 2t_c$. The output corresponding to A_1 appears at V_{OA} at $t = 910t_c$. The output corresponding to B_1 appears at V_{OB} @ $t = 911t_c$. This mode of operation results in an effective sampling rate of twice the rate of ϕ_{1A}, ϕ_{1B}, ϕ_{SA} and ϕ_{SB}.



CCD321A

Stop/Start Mode Operation — The charge packets in the two analog shift registers can be held stationary by stopping ϕ_{1A} and ϕ_{1B} in their LOW state ϕ_{SA}, ϕ_{SB}, ϕ_{RA}, and ϕ_{RB} can also be stopped in the LOW state or kept clocking as usual. The two shift registers should not be connected in series in the stop-start mode of operation.

The CCD321A comes in four different classes depending on the particular application. The CCD321A-1 is basically a high quality broadcast 1 H delay line for video systems with 1% differential gain and 1° differential phase. The CCD321A-2 is a high quality video delay line with 3% differential gain and 3° differential phase. The CCD321A-3 is tested in the START/STOP mode of operation and parameters guaranteed in this mode. The CCD321A-4 is tested at audio speeds and audio type parameters are specified and guaranteed. The dc and clock characteristics of the four classes are the same. The ac characteristics vary as shown below.

Caution: The device has limited built-in gate protection. Charge build-up should be minimized. Care should be taken to avoid shorting pins V_{OA} and V_{OB} to ground during operation of the device.

DC CHARACTERISTICS: $T_A = 55°C$, Note 16

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{DD}	Output Drain Voltage	14.5	15.0	15.5	V	
V_2	Analog Shift Register DC Transport Phase Voltage		6.0		V	Note 1
V_{RA}, V_{RB}	Analog Reference Inputs Voltage		3-7		V	Note 2
V_{GG}	Signal Ground		0.0			
V_{SS}	Substrate Ground		0.0			Note 3
R_{IN}	AC Input Resistance		1.0		MΩ	Resistance from Pins 3, 4, 12 or 13 to V_{SS}. $V_{IA} = V_{IB} = 3$ V
C_{IN}	AC Input Capacitance		10		pF	Capacitance from Pins 3, 4, 12 or 13 to V_{SS}. $V_{IA} = V_{IB} = 3$ V
R_{OUT}	AC Output Resistance		250		Ω	$V_{DD} = 15$ V

CLOCK CHARACTERISTICS: $T_A = 55°C$, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi 1AL}$, $V_{\phi 1BL}$	Analog Shift Register Transport Clocks LOW	0	0.5	0.8	V	Note 4
$V_{\phi 1AH}$, $V_{\phi 1BH}$	Analog Shift Register Transport Clocks HIGH	12.0	13.0	15.0	V	Note 4
$V_{\phi SAL}$, $V_{\phi SBL}$	Input Sampling Clocks LOW	0	0.5	0.8	V	Note 5
$V_{\phi SAH}$, $V_{\phi SBH}$	Input Sampling Clocks HIGH	12.0	13.0	15.0	V	Note 5
$V_{\phi RAL}$, $V_{\phi RBL}$	Output Sample and Hold Clocks LOW	0	0.5	0.8	V	Note 6
$V_{\phi RAH}$, $V_{\phi RBH}$	Output Sample and Hold Clocks HIGH	12.0	13.0	15.0	V	Note 6
V_{IA}, V_{IB}	Input DC Level		3-7		V	Note 2
V_{OA}, V_{OB}	Output DC Level		6-11		V	$V_{DD} = 15$ V
$f_{\phi 1A}$, $f_{\phi 1B}$	Analog Shift Register Transport Clock Frequency	0.02		20	MHz	See Note 17
$f_{\phi SA}$, $f_{\phi SB}$	Input Sampling Clocks Frequency	0.02		20	MHz	See Note 17
$f_{\phi RA}$, $f_{\phi RB}$	Output Sample and Hold Clocks Frequency	0.02		20	MHz	See Note 17
ODM	Output DC Mismatch Between A & B Registers		±1		V	
OAM	Output AC Mismatch Between A & B Registers		±20		%	

CCD321A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
All Pins with Respect to V_{SS}	−0.3 V to 18 V

CCD321A-1 AC CHARACTERISTICS: $T_A = 55°C$. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz. Sampling Rate = 14.32 MHz. Vout ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	5.0			MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			1.0	%	Note 9
Δ ϕ	Differential Phase			1.0	degree	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\,(max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-2 AC CHARACTERISTICS: $T_A = 55°C$. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Vout ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\,(max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-3 AC CHARACTERISTICS: $T_A = 55°C$. Both registers in the multiplied mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Clocks are stopped for 300 μs. Vout ≅ 700 mV after 4.2 MHz low pass filter. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	55			dB	Note 10
SN	Spacial Noise		10.0	20.0	mV	Notes 11, 12
$V_{I\,(max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A

CCD321A-4 AC CHARACTERISTICS: $T_A = 45°C$. For each register, Data Rate = 50 KHz. (See Test Load Configuration, Figure 9)
Vout ≅ 1 V

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	23	25		kHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
THD	Total Harmonic Distortion		0.5	1.0	%	Note 13
S/N	Signal-to-Noise Ratio	60	65		dB	Note 14
$V_{I\,(max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	
RSO	Rate of Average Signal Offset		15		mv/ms	Note 15

NOTES:
1. V_2 level should be 1/2 of the ϕ_{1A} or ϕ_{2A} HIGH level. Adjustment in the range of ±1 V may be necessary to maximize signal bandwidth.
2. Signal charge injection is proportional to the difference V_I and V_R. Adjustment of either V_I or V_R is necessary to assure proper operation.
3. Negative transients below ground of fast rise and fall times of the clocks may cause charge injection from substrate to the shift registers. Anegative bias on V_{SS} of -2.0 to -5.0 Vdc will eliminate the injection phenomenon.
4. $C\phi_{1A} = C\phi_{1B} = 30$ pF = Capacitance with respect to V_{SS}.
5. $C\phi_{SA} = C\phi_{SB} = 10$ pF = Capacitance with respect to V_{SS}.
6. $C\phi_{RA} = C\phi_{RB} = 10$ pF = Capacitance with respect to V_{SS}.
7. Signal Bandwidth is typically 1/3 to 1/2 of the sampling rate. See Fig. 1.
8. Insertion Gain = 20 Log V_{OUT}/V_{IN}.
9. Differential Gain and Differential Phase are measured with Tektronix NTSC Signal Generator (147A) and Vector Scope (520A). See Figure 2.
10. Video S/N is defined as the ratio the peak-to-peak output signal to RMS random (temporal) noise. The peak-to-peak signal is the maximum output level that satisfies the ΔG and $\Delta\phi$ specs. See Fig. 3.
11. In the start/stop mode of operation is recommended that the rise and fall times of ϕ_{1A} and ϕ_{1B} exceed 20 ns to eliminate charge injection.
12. Spacial Noise is the peak-to-peak spacial variation (fixed pattern noise) in the device output after clocks have been stopped. It is usually caused by the variation of leakage current density in the shift registers. Spacial noise is a function of the clock stop period and temperature. See Figure 5.
13. Input Signal = 1 kHz sine wave. See Figure 6.
14. Audio S/N is defined as the ratio of RMS signal to RMS noise at 23 kHz bandwidth. Both are measured with an HP3400A RMS Voltmeter. See Figure 6.
15. Rate of Average-Signal Offset is caused by leakage current in the registers. It is function of temperature. See Figure 7.
16. Devices are tested using the values shown in the typical columns.
17. Devices can be operated beyond 20 MHz without damage. The minimum clock rate can be lower than 10 kHz as shown in Figure 4.

TYPICAL VIDEO PERFORMANCE CURVES

FREQUENCY RESPONSE (FOR SINGLE REGISTER)

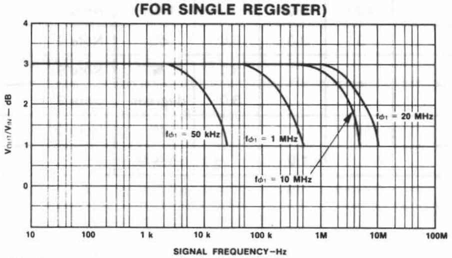


Fig. 1

DIFFERENTIAL GAIN AND PHASE VERSUS OUTPUT VOLTAGE

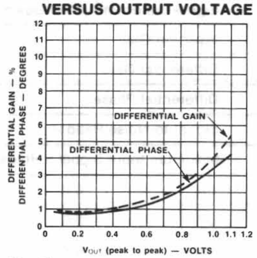


Fig. 2

DIFFERENTIAL GAIN AND PHASE VERSUS S/N RATIO

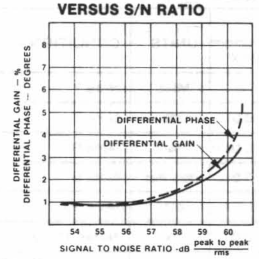


Fig. 3

V_{OUT} MAX VERSUS CLOCK FREQUENCY

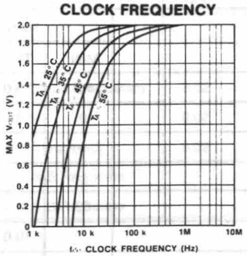


Fig. 4

SPACIAL NOISE VERSUS CLOCK STOP PERIOD

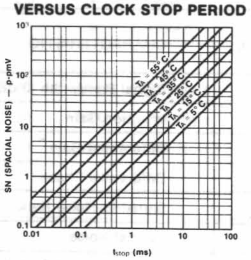


Fig. 5

CCD321A

TYPICAL AUDIO PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION (THD) AND S/N RATION VERSUS V_{OUT}

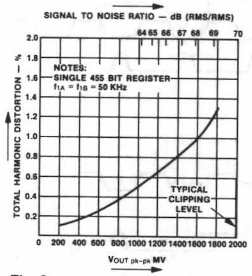


Fig. 6

RATE OF AVERAGE SIGNAL OFFSET VERSUS TEMPERATURE

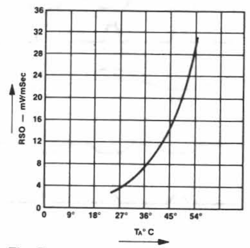


Fig. 7

TEST LOAD CONFIGURATION FOR MULTIPLEXED OPERATION IN VIDEO

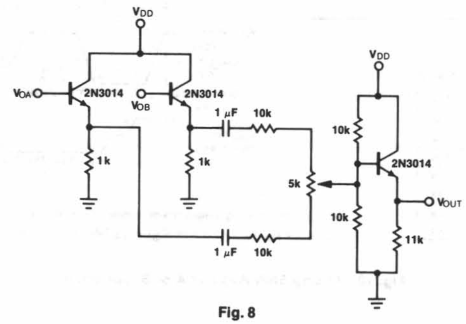


Fig. 8

TEST LOAD CONFIGURATION FOR SINGLE REGISTER OPERATION IN AUDIO AND VIDEO

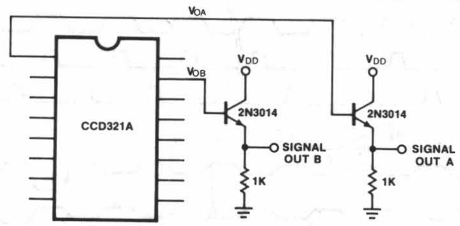
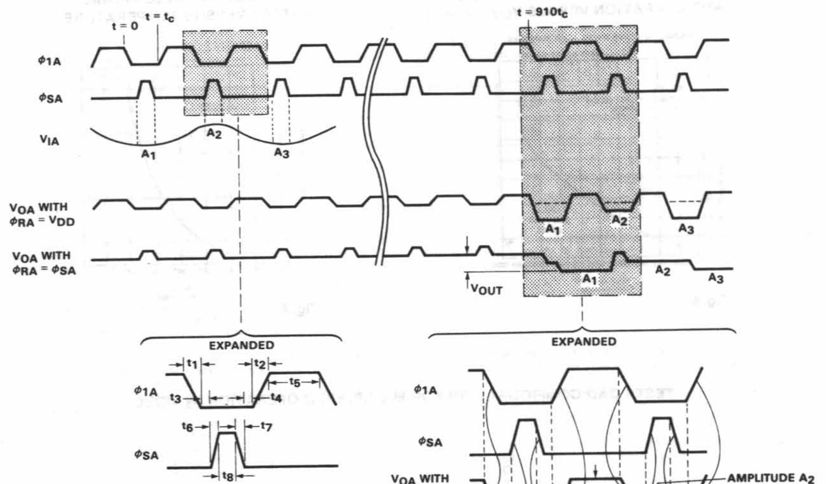
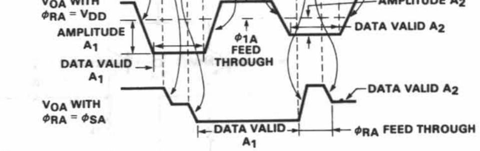


Fig. 9

TIMING DIAGRAM





Timing Requirements for ϕ_{1A} and ϕ_{SA}

TIME	RANGE MIN	TYP	MAX	UNITS
t_1		10		ns
t_2		10		ns
t_3		5.0		ns
t_4		5.0		ns
t_5		15		ns
t_6		5.0		ns
t_7		5.0		ns
t_8		5.0		ns

NOTE:
This timing diagram also applies for shift register B. In this case, ϕ_{1A} becomes ϕ_{1B}, ϕ_{SA} becomes ϕ_{SB}, V_{IA} becomes V_{IB} and V_{OA} becomes V_{OB}.

Fig. 10 Analog Shift Register A or B Operation

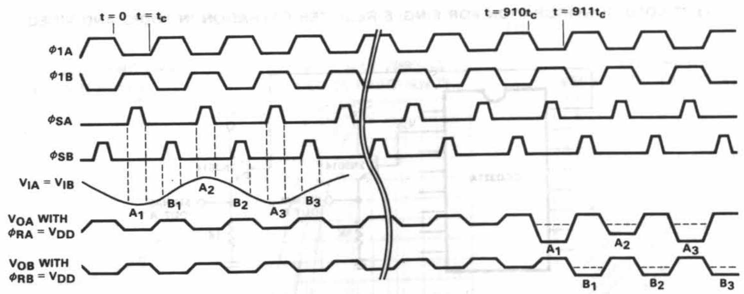
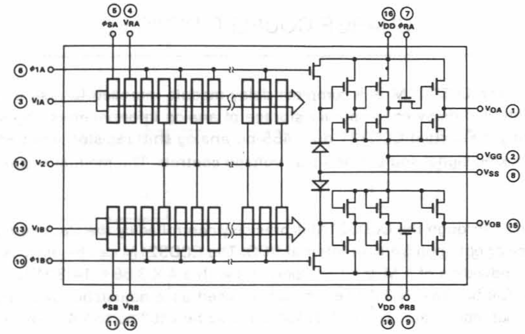


Fig. 11 Analog Shift Register A and B Operation in the Multiplexed Mode

Fig. 12 Circuit Diagram



ORDERING INFORMATION

To order the CCD321A specify the "device type" as shown below:

CLASS, APPLICATION	DEVICE TYPE
CCD321A-1, Broadcast quality video	CCD321A1
CCD321A-2, Industrial quality video	CCD321A2
CCD321A-3, Time base compression and expansion	CCD321A3
CCD321A-4, Audio delay line	CCD321A4

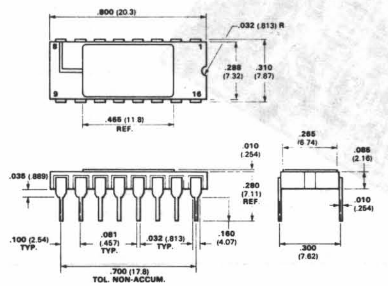
Also available from Fairchild is a fully-assembled module that contains all the necessary circuitry to operate the CCD321A. The module is designed to help the system designer become familiar with the operation of the device, and for use in OEM systems.

The CCD321VM is a video module using a CCD321A-3. The module includes the necessary electronics to perform time base compression and expansion, and variable video signal delay. The module requires a single power supply for operation.

Schematics and component layouts are included in the shipping packages for the CCD321VM. For further information on the CCD321VM please contact your nearest Fairchild sales office or distributor or call 415-962-3941.

PACKAGE OUTLINE

16-Pin Side Brazed



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Header is black ceramic (Al_2O_3)
Pins are gold-plated kovar
Top cover connected to pin 8 (V_{SS} substrate)

CCD321M

VIDEO DELAY MODULE

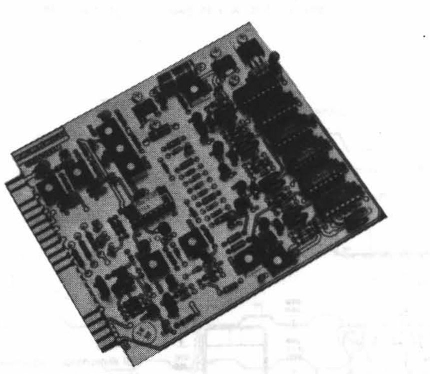
CHARGE COUPLED DEVICE

GENERAL DESCRIPTION – The CCD321M is a complete delay module intended for use in video signal processing systems where precisely controlled delay or temporary storage of analog information is required. The module is a printed circuit board containing a Fairchild CCD321 dual 455-bit analog shift register, input and output signal processing circuitry, and the required clocking signal sources and bias voltage controls. The module requires a single +20 V power supply input for operation.

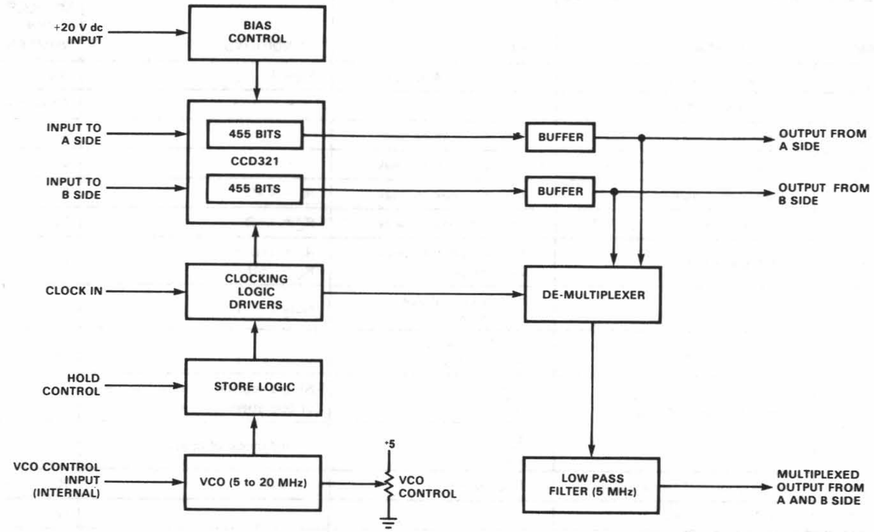
The delay time of analog signals through the CCD321M is precisely controlled by the clock signal frequency which can be provided by an external source or obtained from an internal VCO. The CCD321M can be used as a 910-bit one horizontal line (1H) delay for TV video bandwidths of 5 MHz when operating with a 4 X 3.58 = 14.3 MHz clock frequency,serve as a temperary analog store for a full-bandwidth TV line, or can be used as a adjustable delay by controlling either the internally generated or external input clock. The CCD321M can also be used as two 455-bit registers for delay of two independent analog signals.

Typical video applications for the CCD321M include time-base correctors, video re-synchronising systems, comb filter realizations, moving target indicators and signal-to-noise enhancement systems. Other applications include time-base compression and expansion systems, phase delay equalizers and general purpose analog delay.

- **1 H DELAY LINE PERFORMANCE**
- **ELECTRICALLY VARIABLE DELAY**
- **ADJUSTABLE DELAY – BY CLOCK CONTROL**
- **WIDE SIGNAL BANDWIDTH – 5 MHz**
- **HIGH S/N RATIO – 55 dB**
- **DUAL 455-BIT OR SINGLE 910-BIT DELAY**
- **NO DRIFT – DELAY DEPENDENT ON CLOCK FREQUENCY**
- **INTERNAL OR EXTERNAL CLOCKING**
- **TEMPORARY STORAGE OPERATION CONTROLLED BY A SINGLE TTL INPUT LINE**
- **SINGLE POLARITY POWER SUPPLY – +20 V**



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Dual 455-Bit Analog Shift Register: CCD321

The Fairchild CCD321 is a monolithic 455/910-bit charge coupled device analog shift register packaged in a 16-pin dual in-line package. Functionally this device employs discrete electronic charge packets representing the sampled amplitudes of two analog input voltage waveforms that are transported towards output charge sensing amplifiers by a 1-1/2 phase digital clock signal. An integrated sample and hold output stage provides register output waveforms which are a near-replicas of the signals input to the device 455 periods earlier. (See CCD321 Data Sheet for more details concerning this device)

Clocking Logic and Driver Circuits

The transport and sampling clock pulses required for control of the CCD shift register are generated at TTL levels and then amplified and waveshaped by clock line drivers. A transport and a sample pulse for register A of the CCD321 is triggered by each LOW-to-HIGH transition of the master clock input to the CCD321M; a clock pair for register B is triggered by each LOW-to-HIGH clock input transition. Analog information is thus made to travel completely through both sides of the shift register by 455 complete cycles of the input clock.

Storage Logic

A TTL HIGH level on the Enable input terminal of the CCD321M is synchronized to the transport clock pulses and stops the transport and sampling functions of the register. The analog data in the registers when the clocks are stopped is stored until the Enable line returns LOW, and then transported out in the usual manner.

Signal Processing

Signal inputs to the A and B registers of the CCD321 are gain-controlled by individual potentiometers and then ac coupled through 22 μF capacitors into 100 K Ω loads at the device inputs. Two emitter-followers provide the sampled and held register A and register B output waveforms at a 75 Ω source impedance level.

If the two signal input terminals are connected together, the input data is sampled twice during each clock cycle. Alternate sampled analog bits go in sequence to the two registers of the CCD321. These alternating samples are de-multiplexed at the register output, low pass filtered, and given to a third video output lead. A 910-bit resolution is thus obtained, giving a signal delay of 455 clock periods or 910 clock half cycles. This multiplex operating mode provides 63.5 μs delay for a 5 MHz bandwidth signal using a clock input frequency of 2 x 3.58 MHz = 7.16 MHz, equivalent to a 14.3 MHz sampling and transport rate.

Clock Oscillator

The internal clock generator of the CCD321M is a VCO which can be controlled over a 5 to 20 MHz range by an external 0 to 5 Vdc signal. or adjusted by an on-board potentiometer. An external TTL compatible square wave clock signal can also be used by optional connector wiring.

Bias Control

Power input to the CCD321M is from a nominal +20 V external supply. On-board regulators control bias voltages for the CCD321, drivers, and logic circuitry.

CCD321M

DC CHARACTERISTICS

SYMBOL	PARAMETER	UNIT	CONDITIONS	MODULE PIN NUMBER
V_{CC}	Power Supply Input	+20 Vdc (< 400 mA)	Note 1	A & 1
V_{GG}	Common Ground	0 V	—	All unused pins
V_{IA}	Input to A side of CCD321	500 mV peak-to-peak	—	4
V_{IB}	Input to B side of CCD321	500 mV peak-to-peak	—	6
V_{OA}	Output of A side of CCD321	500 mV peak-to-peak	$R_L = 1\ k\Omega$	8
V_{OB}	Output of B side of CCD321	500 mV peak-to-peak	$R_L = 1\ k\Omega$	10
V_{OM}	Multiplexed Output	500 mV peak-to-peak 300 mV peak-to-peak	$R_L = 1k\Omega$ $R_L = 75\Omega$	12
f_{IN}	Clock In	TTL Square Wave 0 – 25 MHz	Note 2	Z
f_{OUT}	Internal Clock	TTL Square Wave 5 – 20 MHz		22
τ	Input to Output Delay	$\frac{455}{f_{IN}}$	Single register or multiplex mode of operation	
		$\frac{910}{f_{IN}}$	Series mode of operation	
HOLD	Hold Control (Enable Input)	TTL Levels		20
VCO (IN)	VCO Control Input	0 – 5 Vdc		W
VCO(INT)	VCO Internal Control	0 – 5 Vdc		19

AC CHARACTERISTICS: $T_A = 25°C$, Multiplexed Mode of Operation, $f_{IN} = 7.16$ MHz $V_{IA} = V_{IB} = 500$ mV peak-to-peak, $\tau = 63.5\ \mu s$, See Note 3

SYMBOL	PARAMETER	VALUE	CONDITIONS
BW	Bandwidth (3 dB down)	5 MHz Min	
ΔG	Differential Gain	2.5%Max	Note 4
Δφ	Differential Phase	2.5° Max	Note 4
THD	Total Harmonic Distortion	2% Max	Note 5
S/N	Signal to Noise Ratio	55 dB Min	Note 6
T	Tilt of 60 Hz Square Wave	1% Max	
F	Band Pass Flatness: To 3.58 MHz	1 dB	
Offset	DC Offset in Temporary Storage Mode	2.5 mV/ms	Note 7

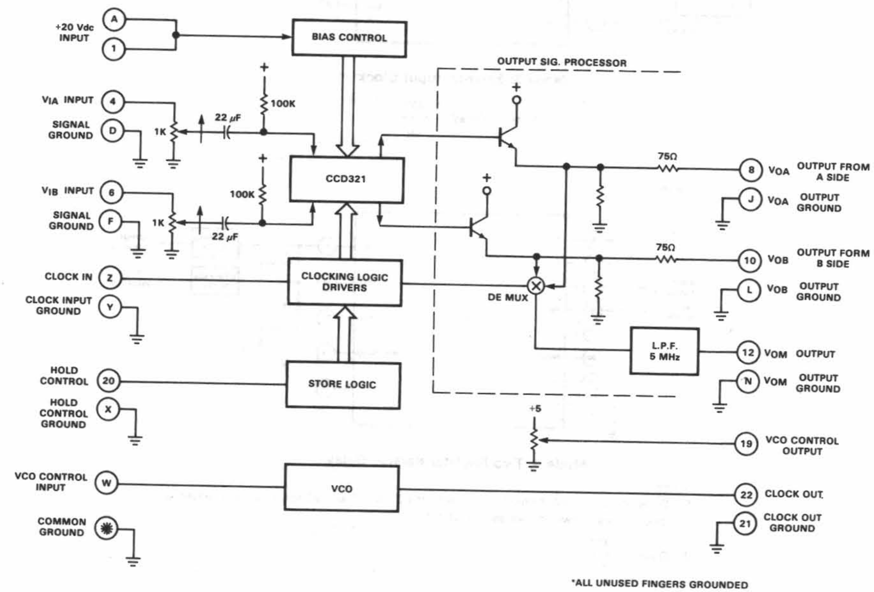
NOTES:
1. Module operates from 19 to 24 Vdc.
2. f_{IN} is the clock of a single register. In the series or independent register mode, a sampling clock of 4X the signal bandwidth is usually required. In the multiplex mode, a sampling clock of 2X the signal bandwidth is required. (i.e, in the multiplex mode of operation, with $f_{IN} = 10$ MHz per side a 5 MHz (3dB) bandwidth can be processed through the device.)
3. AC parameters guaranteed from 0°C to 55°C. Delay tolerances determined by stability of clock frequency.
4. Measured on a Tektronics 520 VECTORSCOPE.
5. Using $f_{IN} = 10$ MHz, multiplexed mode, $V_{IA} = V_{IB} = 500$ mV peak-to-peak, 1 MHz sine wave. Measurement done using spectrum analyzer.
6. Using Rhode and Schwartz noise meter at 4.2 MHz bandwidth.
7. This is a dc offset on the output signal which can occur because of dark current build-up when in hold mode. This offset can be expected to double for each 8-10°C increase in the CCD321 junction temperature.

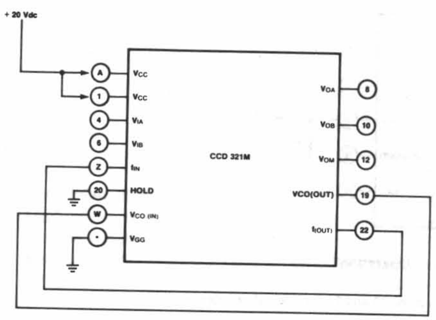
CCD321M

Modes of Operation and Connection Diagrams
The CCD321M can be operated in various modes: (1) Two independent 455-bit analog registers, (2) multiplex, (3) series and (4) temporary analog storage. An on-board generated clock with adjustable frequency, and internal VCO controlled clock or an independent externally generated clock input can be used in any of the four modes.

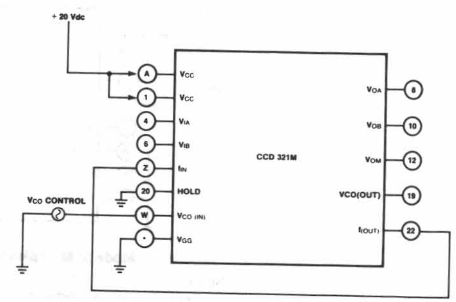
The circuit diagram shown below shows the pin nomenclature for the CCD321M.

The following diagrams represent the correct input/output connections for proper operation of the CCD321M in the various modes. The CCD321M circuit diagram is included in the module shipping package.



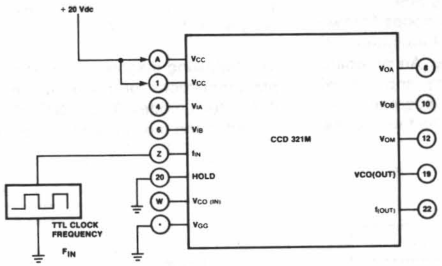


Mode 1: Internal Clock, Adjustable Frequency (R1)



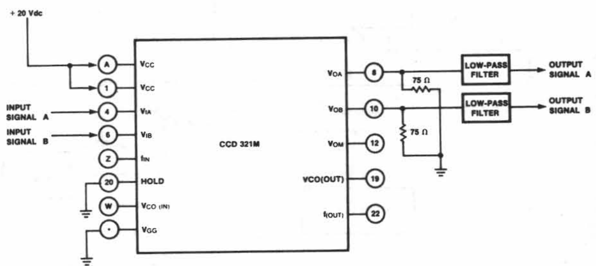
Mode 2: Internal Clock, V_{CO} Input Variable Delay

CCD321M



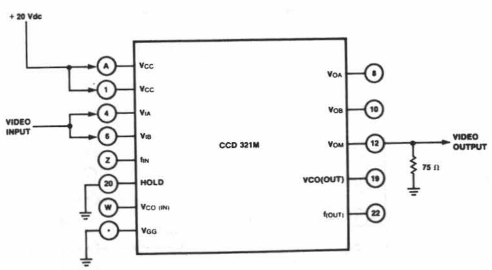
Mode 3: External Input Clock

Note 1: Delay = $\frac{455}{f_{IN}}$



Mode 4: Two Register Parallel Delay

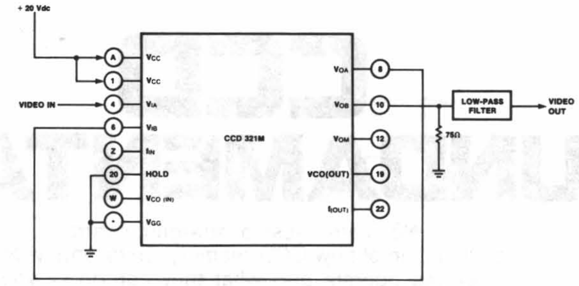
Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{455}{f_{IN}}$



Mode 5: Multiplexed Mode of Operation

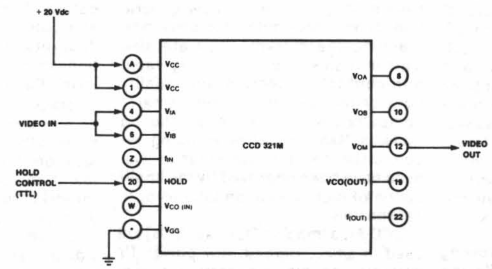
Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2, and 3.
2. Delay = $\frac{455}{f_{IN}}$

CCD321M



Mode 6: Series Mode of Operation

Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{910}{f_{IN}}$



Mode 7: Temporary Analog Storage Operation

Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Store signal (TTL)

MECHANICAL SPECIFICATIONS

1. Module size is 4.5" X 5" X .75" (excluding edge connector).
2. Module weight is 5 oz.
3. Edge connector is 22-pin double readout, .156 center-to-center spacing. Mating connectors can be TRW type 50-44 series edge connector, or equivalent. Wiring information included with each module.

ORDER INFORMATION

To order a CCD321M, contact your nearest Fairchild sales office, representative or distributor. For any technical questions, contact Fairchild at 415-493-8001.

CCD FUNDAMENTALS

No math—just a straightforward explanation of how CCD memory units and video devices operate and what they can do for you!

Charge-coupled devices (CCDs) are a new family of silicon semiconductor components capable of performing the general functions of image sensing, analog signal processing, and digital or analog memory. To realize the CCD concept's full capability, improved LSI techniques have been developed and basic NMOS processes substantially refined. Recognizing the technical advantages of using CCDs in defense systems, military and other government agencies started funding a number of research and development programs in the early seventies to accelerate the development of practical devices.

Today, there is a small but growing number of manufacturers offering high-performance CCD image sensing devices, analog signal processing devices, and large capacity digital memory integrated circuits. Several laboratories are also developing and building small numbers of special devices with government contractual support.

CCD Linear Imaging Devices (LIDs) have made possible the new generation of fast facsimile machines now reaching the market. They are also used in high speed mail sorting, rapid non-contact inspection and quality control measurement, and "smart" computer-controlled material handling systems. Real-time aerial mapping, reconnaissance, and surveillance systems have been improved by the application of high resolution LIDs as optical sensors.

CCD Area Imaging Devices (AIDs) are used in small, rugged, low power TV cameras capable of operation in very low light levels such as one-quarter moonlight. They have been applied in robots and automatic production systems as well as in miniature TV cameras for military systems (Figure 1).

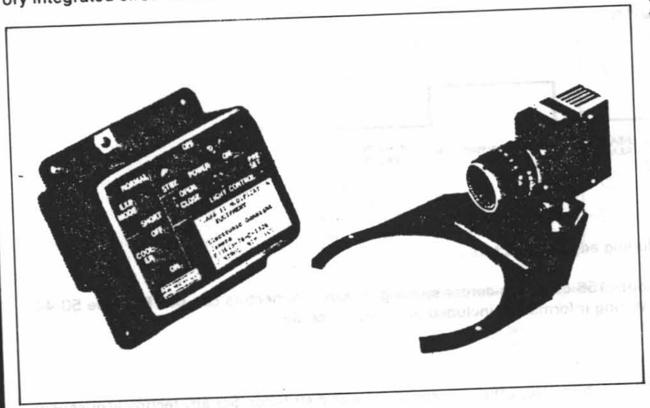


Figure 1: Cockpit TV camera system.

The Charged-Coupled Device

The CCD operating principle is called "charge-coupling." Finite amounts of electrical charge called "packets" are created in specific locations in the silicon semiconductor material. Each specific location, called a "storage element," is created by the [illegible]d of a pair of gate electrodes very close to the surface of the silicon at that location. By placing the storage elements adjacent to each other, in a line for instance, voltages on the adjacent gate electrodes can be alternately raised and lowered and cause the individual charge packets beneath them to be passed from one storage element to the next (Figure 2). Since each charge packet may be of different size, the line of elements becomes a very simple analog shift register. All CCDs are basically shift registers, and because the transfer of charge from each storage element to the next adjacent element is very efficient, the amount of charge in each packet stays substantially the same, even after it has been passed from one element to as many as a thousand sequentially adjacent elements. Since the amount of charge in each packet is unique, the string of charge packets can represent analog information. The device is, in a sense, storing that information until it is delivered as an electrical signal from the charge detector built into the device at the end of the charge-coupled register.

This shift register performance is the basic characteristic of CCDs used in analog signal processing and memory devices. Figure 3 shows a diode-gate structure by which information is put into and taken out of the CCD register to allow operation in an electronic system operating with currents and voltages rather than with the charge-packets manipulated in the CCD itself.

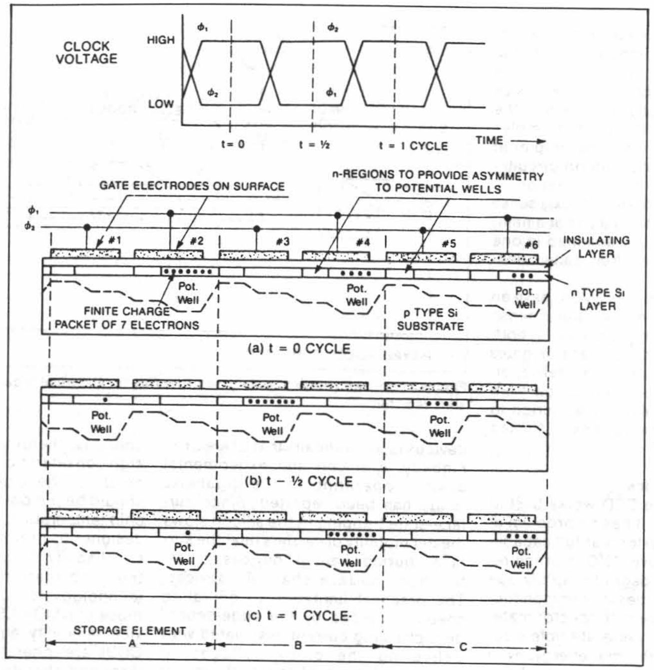


Figure 2: A two-phase CCD shift register. The two complementary clock voltage waveforms ϕ_1 and ϕ_2 are connected to alternate closely-spaced gate electrodes on the surface of the thin insulating layer on the silicon. A deep potential well which attracts electrons is created under the electrode clock voltage HIGH and disappears under the electrodes at clock voltage LOW. At t = 0, ϕ_2 voltage is HIGH and the finite charge packet of seven electrons is in the potential well under gate electrode #2 in storage element "A". At t = ½ cycle later, the potential well under gate #2 has collapsed due to ϕ_1 having gone LOW, and, since at the same time the adjacent electrode #3 connected to ϕ_2 has gone HIGH, the seven electron charge packet has been attracted to the new potential well under electrode #3. Another half cycle later, at t = 1 cycle, the potential well under electrode #3 has collapsed with ϕ_2 going LOW and the electron packet moves to the new well under electrode #4 which has gone HIGH with clock voltage ϕ_1.

Performing the image sensing function utilizes another basic characteristic of silicon semiconductor devices. This is the photoelectric effect by which free electrons are created in a region of silicon illuminated by photons in the approximate spectral range of 400 (blue) to 1100 (near infrared) nanometers wavelength. Response peaks at about 800 nanometers. Absorption of such incident radiation in the silicon generates a linearly proportional number of free electrons in the specific area illuminated. If a silicon device structure having a repetitive pattern of small but finite photo-sensing sites is created, the number of free electrons generated in each site (charge-packet) will be directly proportional to the incident radiation on that specific site. If the pattern of incident radiation intensity is a focused light image from an optical system viewing a scene, the charge-packets created in the finite photo-sites array will be a faithful reproduction of the scene projected on its surface.

After an appropriate exposure time, during which the incident light on each site is generating its time and intensity proportional electron charge-packet, the charge-packets are simultaneously transferred by charge-coupling under an adjacent single long gate-electrode, to a parallel CCD analog transport shift register. The single long gate is called the transfer-gate (Figure 4).

Each charge-packet corresponds to a picture element (pixel) and, when transferred to the adjacent CCD transport shift register, continues to faithfully represent the total sensed radiant energy which was absorbed in the specific photo site. The transfer gate is immediately returned to the non-transfer clock level (LOW) so photo-sites can begin integrating the next line of incident image information. At the same time, the CCD analog transport register, now loaded with a parallel-transferred line of picture information in the form of charge-packets from a line of sensor sites, is rapidly clocked to deliver the picture information, in serial format, to the device output circuitry.

The output circuitry consists of an output gate-diode structure and appropriate reset and buffering signal amplifiers. The output terminal delivers a sequence of electrical pulses, the amplitude of each being directly proportional to the charge-packet size generated in the photo-site where the charge-packet originated. Sample-and-hold circuitry, either on-chip or in the video processing support circuitry ivers a line of video information.

Linear imaging devices (LIDs) sense and deliver information a line at a time; they are electronically scanned in one dimension and are often called line-scan devices.

Area imaging devices (AIDs) have an X-Y array of sense elements and sense an area image. They are built with both vertical and horizontal transfer gates and transport registers, and deliver an entire field of video information from each integration (exposure) period in the form of a series of lines of video signal.

CCD Characteristics

• Temperature: the CCD works best at low temperatures. It has no problem at −55°C and can perform at full capability to +70°C. Above 70°C, storage-related parameters degrade rapidly due to physical properties of semiconductor materials. All semiconductor materials continuously generate hole-electron pairs due to thermal energy, even at room temperature. If there is a finite packet of electrons representing information in a storage element, and thermally generated electrons add to at packet over a period of time, the ..acket will become larger and eventually will no longer accurately represent the original information.

In image sensors, which are very high dynamic range analog devices, it is often desirable to provide cooling for low light level applications to reduce thermal electron generation. Since image sensor devices are used as single units or as a matrix of two to six devices, and dissipate on the order of 150 mW or less, cooling is relatively simple. In CCD memory, long registers could be a problem, so the devices are designed with "refresh" cells at frequent intervals in the register. These sense-and-restore cells detect the "1" or "0" at the output end of a shift register section before enough thermal electrons can be added to cause misinterpretation of the data. Practical economic considerations, however, limit the temperature range for CCD memory to about −70°C. Because of the very low power dissipated in CCD memory, it is practical to consider providing cooling to achieve economical military electronic systems.

• Speed: the speed limitation of CCD devices is theoretically that of electron mobility in silicon and experimental devices operating in the gigahertz range has been reported. Since surface-state trapping in the silicon slows the net mobility of carriers near the surface, "buried channel" devices are faster than "surface channel" devices. The practical limitation to operating speed is caused by the edge-dependent charging current associated with delivering the clock voltages to the capacitances of the shift-register gate electrodes (C dv/dt current). The clock-driver circuitry also dissipates increased power with increasing frequency of operation. Desired operating speed is, therefore, a very strong design consideration in determining how much of the clock driving function should be put on-chip, thus increasing chip temperature, or left for the system designer to provide on the board.

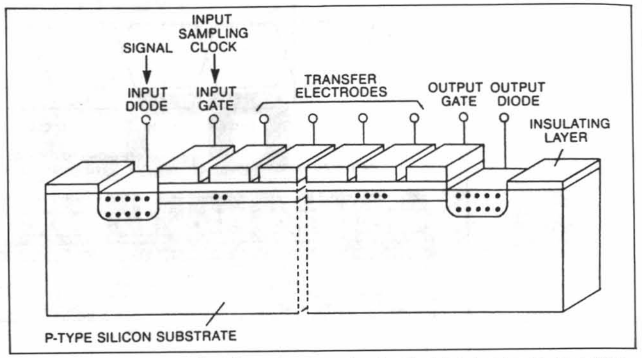


Figure 3: Input and output diode/gate structures for electrical input and output to a CCD shift register.

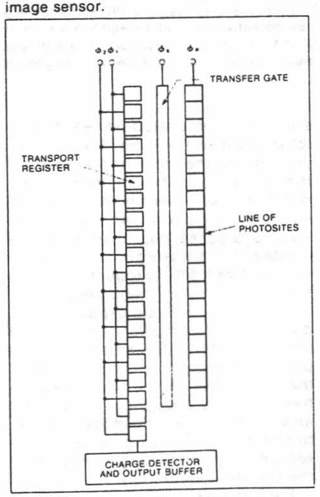


Figure 4: Simplified block layout of a linear image sensor.

• Reliability. Since materials used and the rabrication and packaging technology for CCDs are essentially those of NMOS LSI products, CCD device reliability equals that of NMOS. CCDs are inherently lower power devices and, therefore, the occurrence of thermally-induced failure mechanisms should be lower than that of NMOS. Manufacture of CCDs utilizes state-of-the-art NMOS production technology for its N channel, silicon gate, ion-implanted, surface passivated structure. Packaging can be in any of the commercial or high-reliability packages already proven in industry.

• Noise. The basic CCD register, heart of all CCD devices, is practically noiseless because it does not have PN junctions as do MOS and bipolar devices. Associated on-chip charge detectors and buffer amplifiers do have PN junctions and introduce some noise. Dynamic ranges of 10,000:1 have been achieved with cooling; 200:1 to 500:1 is common at room temperature.

• Radiation Hardness. CCDs are not basically "hard." They are fabricated on very lightly doped, high-resistivity silicon which has characteristics more easily altered by radiation than the more heavily doped silicon in bipolar and conventional MNOS devices. Buried channel CCDs have been reported to be more radiation tolerant than surface channel devices. Government sponsored development programs are under way at several laboratories to investigate methods for radiation hardening CCD devices.

.245" × .245". AIDs applications include:

• Low light level search and surveillance
• Missile and RPV guidance
• Star tracking
• Remote or projectile TV reconnaissance (Figure 5)
• Cockpit or gunsight camera
• Space telescope

Large area AIDs are difficult to produce "blemish free" at low cost. Industry is aggressively addressing reduction and elimination of random defects to achieve practical, low-cost volume-producible AIDs with chip diagonal dimensions in the order of 0.500".

Analog Signal Processors

The CCD has been shown to be a nearly ideal analog shift register. The simplest analog signal processor is a variable analog delay line where the delay obtained is a direct function of the clocking frequency and the number of storage elements in the register. Differential phase and differential gain of 1% or less is available in commercial devices. Tapped CCD delay lines are excellent sampled analog filters and can be externally programmed to change filter characteristics, scan a frequency spectrum, or provide correlation of weak signals in a strong noise background. CCD Analog Signal Processor applications include:

• Video and audio variable delay lines
• Moving target indicator filter
• Signal correlation and convolution
• Sonic imaging
• Voice compression and scrambling
• Video frame-grabber
• Communications and secure communications filter
• Scan rate converter
• Spread spectrum filter

Digital Memory

All CCD memories are basically serial because of the fundamental shift register nature of charge-coupling. They are dynamic memories which require periodic refreshing and, like other semiconductor memories, they are volatile. While their latency is greater than bipolar and MOS memory, they are as much as fifty times faster than magnetic disc and drum memories. Because of the shift-register nature of CCD, the CCD memory devices are block-access oriented rather than random bit accessed. The high bit-count per package allows use of distributed memory and changes in computer architecture. CCD memory applications include:

• Cache memory
• Bulk storage
• Signal analysis for sonar, radar
• Synthetic aperture radar memory
• Digital delay
• Drum and disc replacement

As manufacturing technology continues to improve, all semiconductor memory will enjoy an increase in bit-density and a reduction in device and system costs due to the reduction in package count. CCD memory specifically will continue to remain more dense than bipolar and MOS memory for reasons previously stated. It is probable that CCD memory, because of its lower power dissipation, will be able to shift to packaging capable of being mounted more densely on P.C. boards. It is also probable that power dissipation can be reduced further by designing for operation at lower voltages. Peripheral circuitry such as on-chip drivers will be added to new CCD memory devices to the extent that added power dissipaiton can be tolerated and the additional silicon area required is economical from an overall systems cost standpoint.

Conclusion

Charge-coupled devices are now a family in production, bringing new capability to the military electronics systems designer. The high-volume, low cost production of area image sensors for TV sensing will require a combination of elimination of the causes of random defects from each step in the manufacturing process and improvement in the photo-lithographic techniques for patterning large area arrays so their area can be reduced without reducing responsivity.

Volume production of high performance analog signal processing devices such as filters requires definition of a volume market sufficient to warrant the development costs and application of resources. Increased control of manufacturing processes, particularly accuracy of the photo-lithographic process or its electron-beam successor, will allow the dimensional control necessary to produce devices which are linear over a large dynamic range and have the high rejection characteristics desired.

CCD memory will move ahead in the next few years to 256K bits per package from the present 64K level. Further, reduced power dissipation per bit and more compact packaging are probable.

• Packing Density. CCDs have a three to five times packing density advantage over the next most dense MOS large-scale-integrated circuits. This is primarily because the basic CCD storage element requires no electrical contacts. The storage and transport of the information in the CCD register are performed by the pattern of conductive gate electrodes on the surface of the thin oxide layer over the silicon. The gates require much less area per storage element than the combination of gates and ohmic contacts required for an MOS storage element. The 64 kilobit CCD memory device presently produced by Fairchild is a chip of silicon .175" × .230" in size.* With foreseeable improvements in LSI manufacturing technology and careful selection of the memory chip organization and on-chip peripheral circuits, devices with 256 kilobits capacity will be available within the next year or two.

CCD Applications in Miliary Electronics

Image Sensors. A CCD image sensor device can be configured as a line-scan device or as an X-Y TV type device. It can also be configured as a combination of the two basic structures for special applications. The line-scan device has a single line of sense elements and scans itself electronically in one axis—along the sense elements' centerline. It is often referred to as a Linear Imaging Device (LID). The X-Y device is an area matrix of sense elements capable of being electronically scanned in both X and Y axes to produce an area TV picture. It is often referred to as an Area Imaging Device (AID).

Most CCD image sensors have wide spectral range, and are nominally useful over the spectral range 450 to 1000 nanometers; i.e., visible through the middle of the near infrared regions. Standard commercial CCD image sensors will operate well up to a wavelength of about 800 to 900 nanometers; beyond that wavelength, they lose resolution rapidly. Resolution loss is due to the IR image photons generating electrons much deeper in the silicon and, therefore, beyond the attractive effect of the field created by the gate electrodes at the silicon surface. The generated electrons diffuse in the bulk of the silicon until they are either lost by recombination or move nearer to the surface where they are captured in the field of one of the sense elements. However, because of the time delay, they may arrive too late or in a sense element other than the one through which their exciting photon entered the silicon. The practical result is a loss of resolution or smearing of the image sensed. In some laboratories, work is being done to develop special CCDs for long wavelength IR image sensing.

All CCD image sensors consume low power and operate on low voltages. They do not exhibit lag or memory and are not damaged by intense light. Present devices will over-saturate and "bloom" under intense illumination but are not permanently damaged. Anti-blooming structures are under development.

Linear Imaging Devices(LIDs)

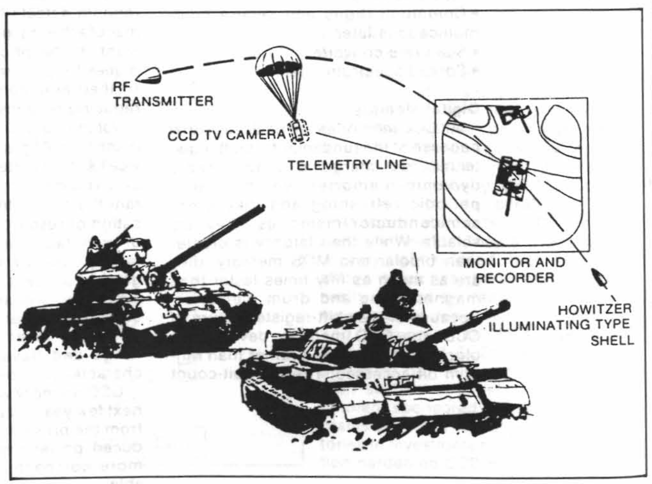
LIDs are configured as a single line of sensor elements on a long narrow chip. These devices are commercially available with 256, 1024, and 1728 elements with longer devices in development. LIDs are used in facsimile machines or spectrometers where the subject is a line pattern. When relative motion of the scene with respect to the sensor is provided by other means, the array can present a high-resolution TV-type picture. A continuous real-time picture can be obtained from a LID sensor in an aircraft or satellite passing over the surface of the earth at a constant altitude and velocity. Using a scanning mirror in the optical system can accomplish a similar result. LIDs applications include:

- High speed, high resolution facsimile (text, maps, fingerprints, photographs)
- Aerial mapping with high measuring accuracy
- Real-time reconnaissance and surveillance
- Bar-code reading
- Sorting parts, mail, currency, food
- Conveyorized product non-contact inspection
- Automatic warehouse routing and palletizing control

Special configurations of LID in which the array is eight to 64 elements wide (rather than one element wide) can be used for Moving Image Integration (MII) applications and are particularly effective in very low light level applications. Combined with analog delay lines, a LID can be used as the sensor for Moving Target Indication (MTI).

Area Imaging Devices (AIDs)

AIDs produce a TV picture. They are built in an array capable of being self-scanned in both the X and Y direction. These devices are available in 100 × 100 element and 244 × 190 element arrays; they have also been built in smaller sized arrays and in arrays of 400 × 400 and 488 × 380 elements. As an example of a commercially available device, the Fairchild CCD211 is a 244 × 190 element array with a sense area format equivalent to a Super 8 movie frame, and in a 3 × 4 aspect ratio for TV presentation. The device dissipates 100 mW when operated at a 7 MHz data rate, and operates at voltages of 12V to 15V. Its dynamic range is typically 300:1 at room temperature. Chip size is



CHARGE-COUPLED DEVICES

The products of a new concept in semiconductor electronics, they hold considerable promise in applications as diverse as image sensors and information-storage elements for computer memories

For the past four years there has been a growing excitement among solid-state physicists about a new concept in semiconductor electronics that may someday have an impact on our lives as dramatic as that of the transistor. The new concept is charge-coupling and its practical manifestation is the charge-coupled device.

Like the transistor, the charge-coupled device is a concept of semiconductor electronics; as such it is subject to the same physical laws that govern the transistor's dynamics and fabrication. That, however, is where the similarity ends. Although the charge-coupled device shares much the same technological base with its distinguished predecessor, it is a functional concept that focuses on the manipulation of information rather than an active concept that focuses on the modulation of electric currents. Transistor technology has made possible computer-memory components with thousands of memory elements on a single chip of silicon; charge-coupling is making possible comparably sized memory components with tens of thousands or even hundreds of thousands of memory cells per silicon chip at approximately the same cost.

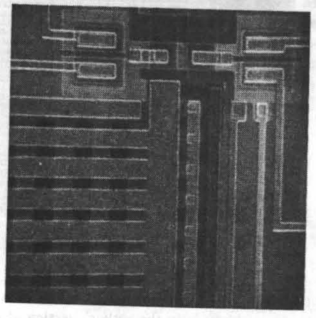
What is charge-coupling? It is the collective transfer of all the mobile electric charge stored within a semiconductor storage element to a similar, adjacent storage element by the external manipulation of voltages. The quantity of the stored charge in this mobile "packet" can vary widely, depending on the applied voltages and on the capacitance of the storage element. The amount of electric charge in each packet can represent information.

Perhaps the easiest way to visualize the operation of a charge-coupled device is through the use of a mechanical analogy. Imagine a machine consisting of a series of three reciprocating pistons with a crankshaft and connecting rods to drive them [*see top illustration on next two pages*]. On top of one or more of the pistons is a fluid. Note that rotating the crankshaft in a clockwise manner causes the fluid to move to the right, whereas rotating the crankshaft in a counterclockwise manner would cause the fluid to move to the left. Since it takes three pistons to repeat the pattern, this arrangement is called a three-phase system. If it is desired to move the fluid in one direction only, a two-phase system can be devised by imposing an asymmetry on the piston design [*see bottom illustration on next two pages*]. Regardless of the direction of rotation, the fluid now advances to the right.

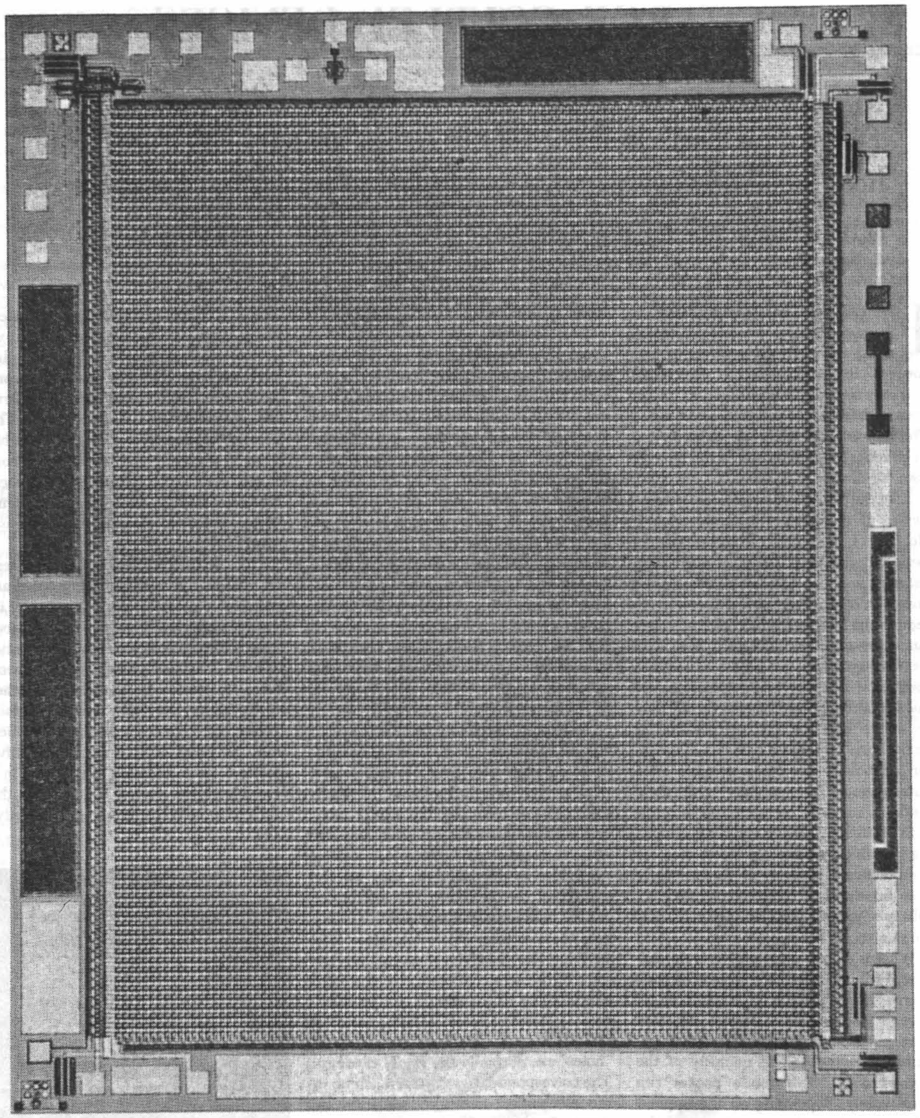
Analogous charge-coupled devices can be fabricated of silicon [*see illustrations on page 26*]. The devices consist of a "*p* type" silicon substrate (in which electrons are normally the signal carriers) with a silicon dioxide insulating layer on its surface. An array of conducting electrodes is deposited in turn on the surface of the insulator. The electrodes can be interconnected to establish either two-phase or three-phase operation. Underlying the insulator and within the bulk of the semiconductor the electrical conductivity of the silicon can be selectively altered to form "*n* type" material (in which not electrons but electron "holes" are normally the signal carriers). The correspondence with the machine in the mechanical analogy is realized by supposing that the fluid represents an accumulation of electrons, that the pistons represent the potential energy associated with the voltages applied to the electrodes and that the crankshaft and connecting rods represent the driving voltages and their relative timing.

When a periodic wave form called a "clock" voltage is applied to the electrodes, some of the electrons in the vicinity of each electrode will form a discrete packet of charge and move one charge-coupled element, or unit cell, to the right for each full clock cycle. The packets of electron charge therefore move to the right as a result of the continuous lateral displacement of the local "potential well" in which they find themselves. They are thus—or so it seems—always falling.

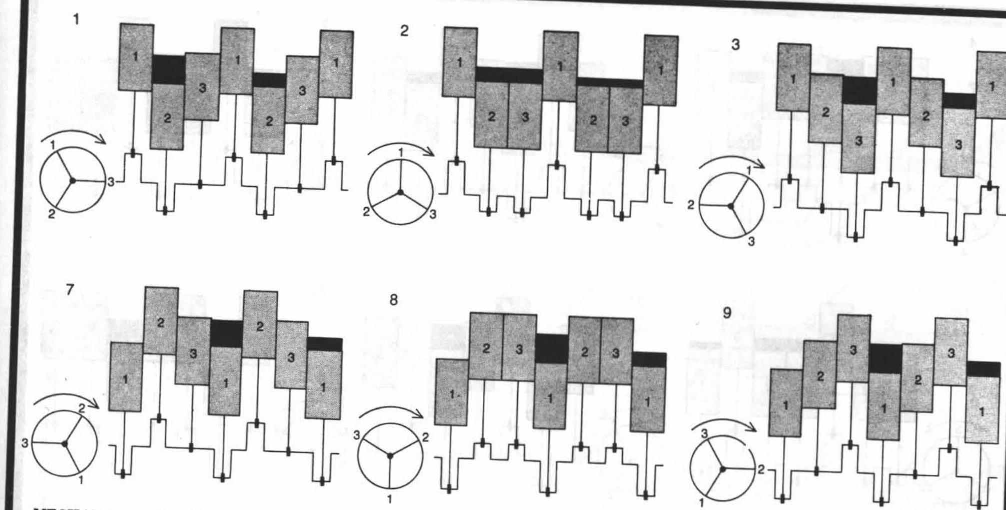
The creation of the necessary potential well in the semiconductor substrate deserves some elaboration because of its central importance to the charge-coupling concept. In this context a potential well is a localized volume in the silicon that is attractive to electrons; in other words, it is the most positive place around and hence is a desirable location from the point of view of the negative electron. Potential wells are formed in a charge-coupled storage element by the interaction of the different conductivity-



CLOSEUP VIEW of a small portion near the output of a charge-coupled photosensor array is provided by this scanning electron micrograph. Each element and its associated readout electrode measure 1.9 square mils.



CHARGE-COUPLED IMAGE SENSOR shown in this color photomicrograph, made in the author's section of the Research and Development Laboratory of the Fairchild Camera and Instrument Corporation, consists of 10,000 photosensor elements arrayed in a rectangular 100-by-100 grid on a silicon chip measuring only .12 by .16 inch. (Large brown and white shapes around border are metal contacts for electrodes.) The device is designed to be used in an experimental television camera based on the concept of charge-coupling, that is, the collective transfer of all the mobile electric charge stored within a semiconductor storage element to a similar, adjacent storage element by the external manipulation of voltages. Although such charge-coupled image sensors are still in a somewhat primitive state, in the author's view they "clearly point the way toward a powerful camera technology." An enlargement of a small portion of a similar charge-coupled photosensor array appears in the scanning electron micrograph on the opposite page.



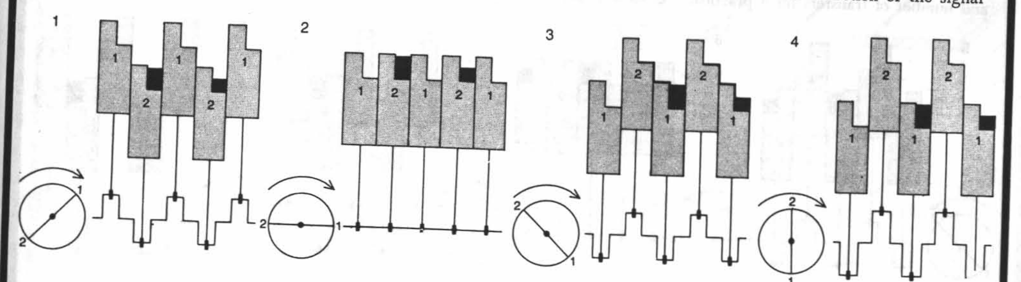
MECHANICAL ANALOGY useful in visualizing the operation of a charge-coupled device is depicted in this sequence of idealized drawings. The machine illustrated consists of a repeating series of three reciprocating pistons with a crankshaft and connecting rods to drive them. On top of one or more of the pistons is a fluid (*color*). Rotating the crankshaft in a clockwise manner, as shown

type regions of the silicon [*see illustration on page 27*]. This interaction forms a well for electrons such that the higher the clock voltage, the deeper the well. Any electrons in the well will move with the clock voltages.

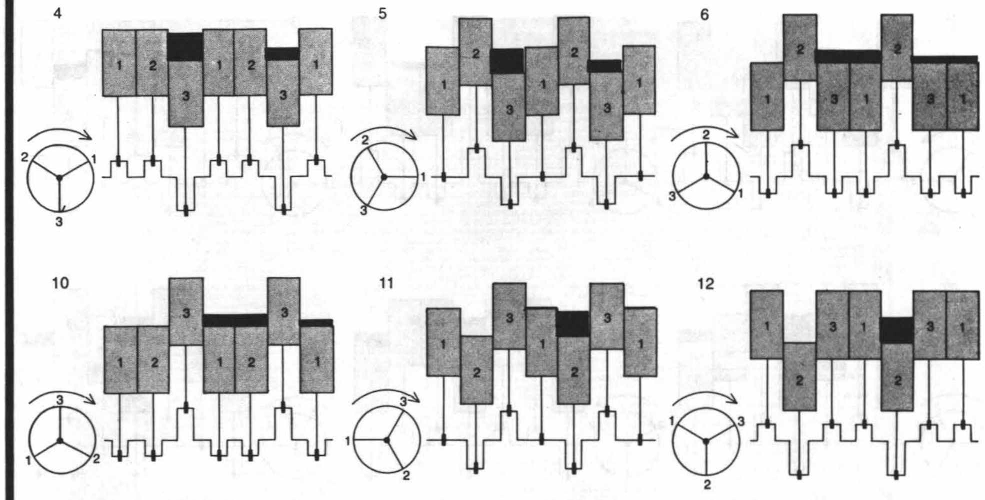
Now, if two or more wells of different depths are placed close to one another, the wells will overlap and charge may be "coupled," or transferred, from one storage element to the next as the depth of the well is altered by the clock voltages. Thus the external clock voltages on the electrodes cause the electrons to move in packets through the semiconductor in a potential-energy trough known as a channel. This mode of electron transfer is the essence of charge-coupling.

The phenomenon of charge-coupling is in itself inadequate for the purpose of constructing a useful device. A practical charge-coupled device must be able to introduce the necessary electrons into the structure and also have a means at some location in the channel for detecting the amount of charge in a packet. Thus for a structure to be classified as a charge-coupled device it must possess at least three attributes: input, charge-coupling and output.

As an example of a simple yet functionally complete charge-coupled device, consider a "shift register" consisting of eight three-phase elements, an input diode and gate and an output diode and gate [*see illustration on page 28*]. This structure is in fact very similar to the first charge-coupled device ever fabricated. The signal that is to be entered into the charge-coupled device is connected to the input diode, which acts as a source of electrons. If the input gate is held at a low voltage, no signal electrons can enter the channel. In order to put a packet of electrons into the device it is necessary to wait until the first-phase electrodes are in the high-voltage condition and then "turn on" the input gate by raising its voltage. Electrons fill the potential well until the energy level for electrons in the well is the same as that for the electrons in the source. The input-gate voltage is now lowered to isolate the source, and the charge packet created is ready for transfer down the channel. In the detection of the signal



ASYMMETRICAL PISTONS are added to the mechanical analogue in order to introduce the operating principle of a two-phase system. Regardless of the direction in which the crankshaft is rotated, the fluid now advances to the right. In the correspondence



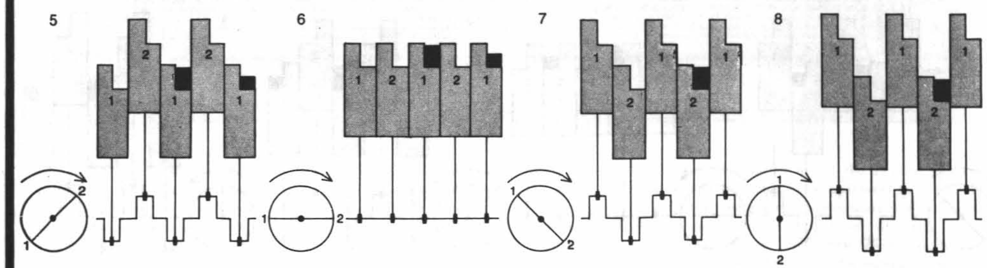
in this instance, causes the fluid to move to the right. If the crankshaft were to be rotated in a counterclockwise manner, on the other hand, the fluid would move to the left. This particular type of arrangement, which requires three pistons to repeat the pattern, is called a three-phase system. An analogous charge-coupled device can be fabricated of silicon (*see top illustration on next page*).

the charge is merely transferred to a "drain," or output diode, where it appears as a current in some external circuit. This simple charge-coupled device fulfills the function of an eight-bit shift register, a device potentially useful in computer architecture.

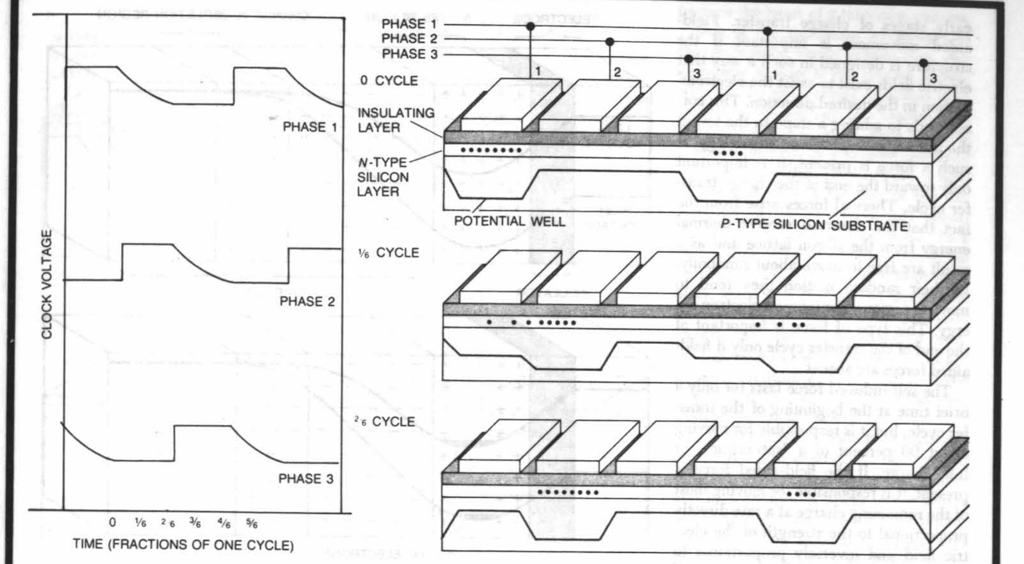
Devices fabricated and operated in this manner verify the predicted performance with one exception. Unfortunately not all the electrons advance with the packet on each transfer, and the residual charge appears in a trailing packet. The magnitude of such "charge-transfer inefficiency" is a function of the design of the device and the frequency of operation. Transfer inefficiency imposes a fundamental limitation on the speed and number of transfers for a practical charge-coupled device because of the resulting attenuation of the charge packet as it is moved through the device from one region to the next.

There are two reasons for charge-transfer inefficiency. First, the electrons may be inhibited from moving because of local regions of lower potential energy (corresponding to dents or ridges in the top of the piston in the mechanical analogy). Second, the frequency of operation may be so high that there is not enough time for all the electrons to follow the moving potential wells. The former problem is one that is influenced predominantly by the design details of the particular charge-coupled device. Researchers working on the development of such devices are continuing to explore this aspect of charge-coupling. Recent advances in technology have significantly reduced the seriousness of the problem. The problem of the speed of the electrons' motion, however, has more basic origins and deserves additional comment.

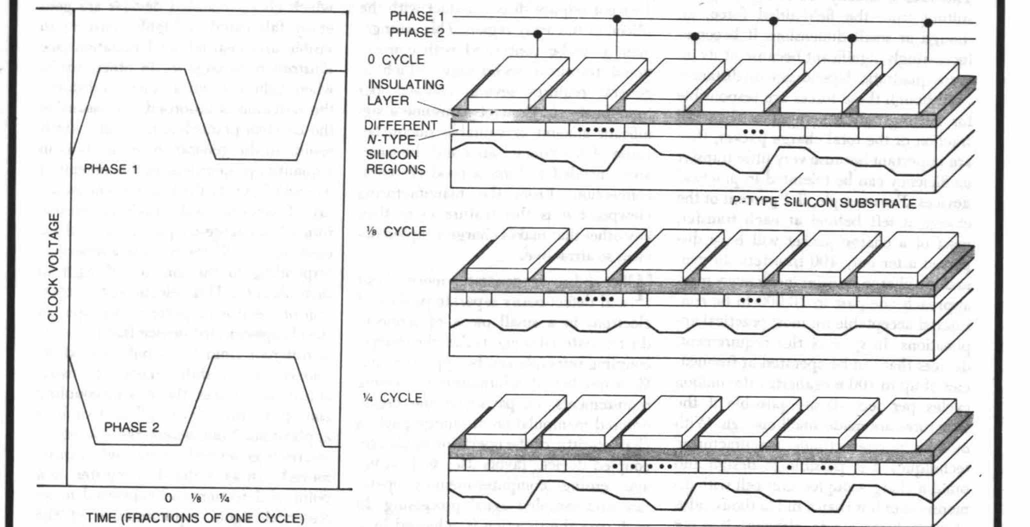
The electrons are induced to move to an adjacent region of lower energy (that is, a deeper potential well) by a combination of three influences: self-induced forces, field-aided forces and thermal forces. Self-induced movement results from the simple fact that a high-density packet of electrons (or any similar particles) tends to spread rapidly if the constraining force is removed, as is the case when the clock voltages change. This type of force is important during the



with an actual charge-coupled device the fluid represents an accumulation of electrons, the pistons represent the potential energy associated with the applied voltages and the crankshaft and the connecting rods represent the driving voltages and their timing.



TWO THREE-PHASE CHARGE-COUPLED ELEMENTS are shown in the cross-sectional diagram at right; the curves at left give the relative timing of the "clock voltage" wave forms for three-phase operation. The device consists of a "*p* type" silicon substrate (in which electrons are normally the signal carriers) with a silicon dioxide insulating layer on its surface. Conducting electrodes are deposited on the surface of the insulator. Underlying the insulator and within the bulk of the semiconductor the electrical conductivity of the silicon can be altered to form an "*n* type" layer (in which electron "holes" are normally the signal carriers). When the clock voltage is applied to the electrodes, some of the electrons in the vicinity of each electrode will form a discrete packet of charge (*black dots*) and move one element to the right for each full clock cycle. In effect the packets of electron charge move to the right as a result of the continuous lateral displacement of the local "potential well" in which they find themselves (*white contours in substrate*).



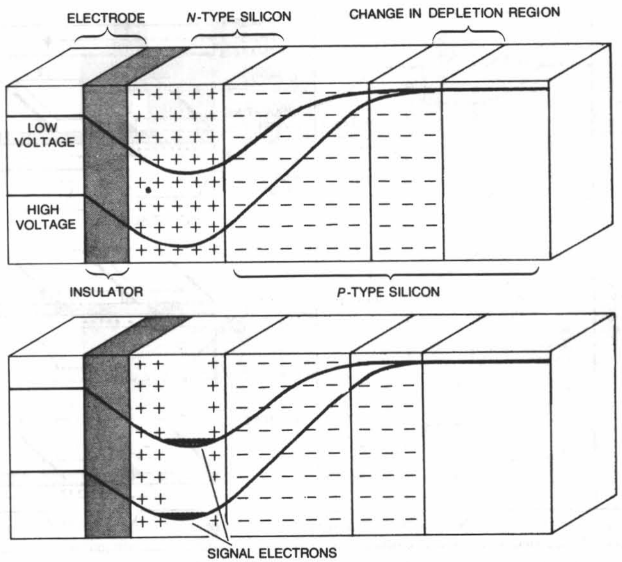
THREE TWO-PHASE CHARGE-COUPLED ELEMENTS are shown in these cross-sectional diagrams; again the curves give the relative timing of the clock voltages, this time for two-phase operation. Here the potential wells are given the required asymmetry by the introduction of different *n*-type conductivity regions just under the insulating layer. As in the illustration at the top, the external clock voltages on the electrodes cause the electrons to move in packets through the *n*-type semiconductor layer toward the right.

early stages of charge transfer. Field-aided movement is important if the structure is designed in such a way that electric fields exist to assist the electrons' motion in the desired direction. This corresponds to adding a slope to the top of the pistons in the mechanical analogy. If such a force is present, it is important only toward the end of the charge-transfer cycle. Thermal forces arise from the fact that the electrons receive thermal energy from the silicon lattice and as a result are free to move about randomly. In their random motion they tend to move to regions of minimum electron energy. This type of force is important at the end of the transfer cycle only if field-aided forces are absent.

The self-induced force lasts for only a brief time at the beginning of the transfer cycle, but it is responsible for moving about 90 percent of a "saturation," or full, charge. If the field-aided force is present, it is responsible for moving most of the remaining charge at a rate directly proportional to the strength of the electric field and inversely proportional to the distance between the electrodes. If the field-aided force is not present, the remaining charge will move under the influence of thermal forces at a rate directly proportional to the temperature and inversely proportional to the square of the distance between the electrodes. This rate is usually lower than that resulting from the field-aided force, although at small dimensions it becomes increasingly significant because of its inverse quadratic dependence on distance.

Although these forces are responsible for moving only a comparatively small fraction of the total charge packet, they are important because very little transfer inefficiency can be tolerated in practical devices. For example, if 1 percent of the charge is left behind at each transfer, most of a charge packet will have dispersed after only 100 transfers. In general the charge-transfer inefficiency must approach one part in 10,000 to be considered acceptable for most practical applications. In spite of this requirement, devices that can be operated at frequencies of up to 100 megahertz (100 million cycles per second) are possible if the structures are made small enough. With modern microelectronic manufacturing techniques it is possible to design and build a charge-coupled unit cell with dimensions of less than a mil (a thousandth of an inch) on a side, although it is not always appropriate to do so.

Unit cells of such small dimensions are possible because of the simple nature of the charge-coupled structure, which

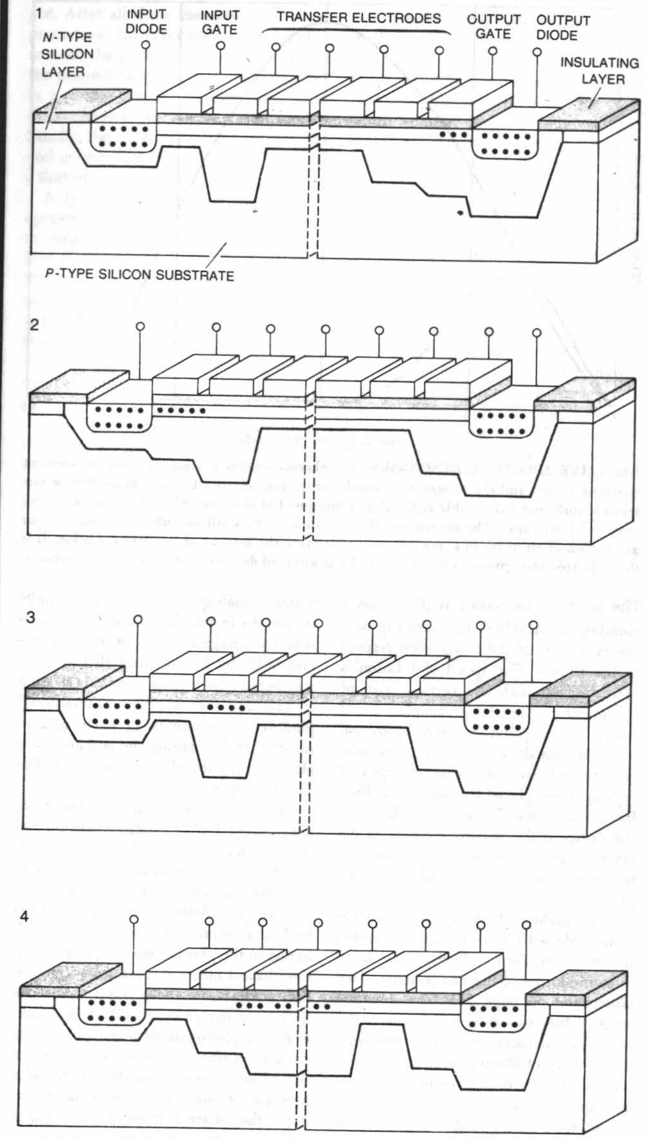


POTENTIAL-ENERGY PROFILES for a typical charge-coupled information-storage element are shown here as a function of distance into the bulk of the semiconductor at right angles to its surface. (In order to show the potential wells clearly, this diagram has been rotated by 90 degrees with respect to the preceding ones.) The charge-distribution patterns are shown for two situations: with no electrons in the well (*top*) and with some electrons in the well (*bottom*). As the curves indicate, the higher the clock voltage, the deeper the well.

does not require direct contact with the silicon in the array region. This arrangement is to be contrasted with conventional transistor technology, which in general requires several contacts per functional cell. Contacts consume a significant amount of valuable silicon because of the contact area and the tolerances needed to form a good electrical connection. From the manufacturing viewpoint it is this feature more than any other that makes charge-coupled devices so attractive.

The ability to generate, move about and detect many separate packets of electrons in a small piece of semiconductor material suggests that the charge-coupling principle can be applied to fulfill a number of information-processing requirements. In particular the highly ordered manipulation of charge packets characteristic of the operation of charge-coupled devices favors uses such as image sensing, computer-memory operation and sampled-signal processing. In each case the function is achieved by a proper combination of charge-coupled unit cells that operate individually exactly as described above.

Silicon, the semiconductor material of which charge-coupled devices are generally fabricated, is highly sensitive to visible and near-infrared radiation [*see illustration on page 9*]. In other words, when light falls on a silicon substrate, the radiation is absorbed (by means of the Einstein photoelectric effect), which results in the generation of electrons in a quantity proportional to the amount of incident light. If there is present an array of potential wells such as the one formed by charge-coupled devices, these electrons will fill the wells to a level corresponding to the amount of light in their vicinity. This "electro-optic" creation of electrons represents an input to the charge-coupled device that is entirely different from the input method required for the shift register discussed above and makes the charge-coupling concept useful for very different kinds of application. Nonetheless, the packets of electrons generated by the light can be moved, just as in the shift register, to a point of detection and converted to an electrical signal representative of the optical image incident on the device. That signal, after some conditioning, can be displayed on a cathode ray tube. In this way a charge-coupled device can



INPUT AND OUTPUT OPERATIONS of a simple eight-element, three-phase charge-coupled "shift register" are summarized in this series of diagrams. The signal enters the device by way of an input diode, which acts as a source of electrons. If the input gate is held at a low voltage, no signal electrons can enter the potential-energy "channel" (*1*). In order to put electrons into the device one must wait until the first-phase electrodes are in the high-voltage condition and then "turn on" the input gate by raising its voltage (*2*). Electrons fill the potential well until the energy level for the electrons in the well is the same as that for the electrons in the source. The input-gate voltage is now lowered to isolate the source (*3*), and the charge packet created is ready for transfer down the channel (*4*). The signal is detected by transferring the charge packet to an output diode, where it appears as a current.

become the heart of a television camera.

One of the significant advantages of charge-coupled image sensors over vacuum-tube sensors is the precise knowledge of the photosensor locations with respect to one another. In a camera tube the video image is "read" from a photosensitive material by a scanning electron beam. The position of the beam is never precisely known because of the uncertainty in the sweep circuits resulting from random electrical noise. In a charge-coupled sensor the location of the individual photosensor sites is known exactly, since it is determined during the manufacture of the component. Such "metric" accuracy is important for proper alignment in color cameras and in applications requiring data reduction of the acquired image (as in photographic missions in space and photogrammetry).

It is generally convenient for purposes of discussion to separate charge-coupled sensors into two categories: linear sensors and area sensors. A linear image sensor is a simple straight-line array of photosensors with the associated readout and sensing circuitry. An area image sensor is a two-dimensional mosaic of photosensors, again with the associated readout and sensing circuitry.

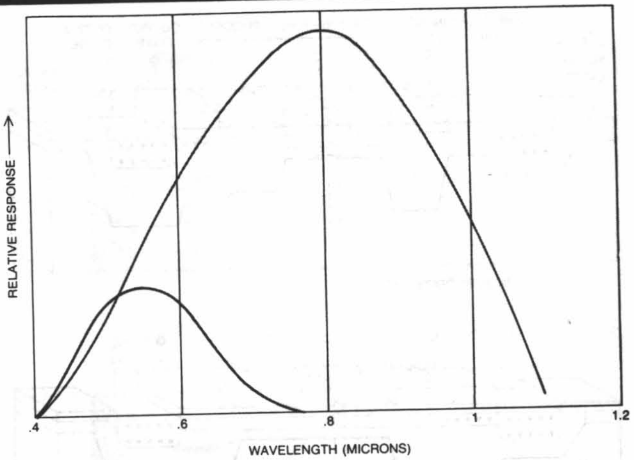
Linear image sensors are used for a host of applications, including air-to-ground and space-to-ground imaging, facsimile recording and slow-scan television. The image to be viewed is obtained by providing relative motion between the sensor and the scene with the axis of the array perpendicular to the direction of the motion. A resolution of 500 or more photosensor elements is usually required. A primitive linear imaging device can consist of nothing more than a charge-coupled shift register and an output diode. In this structure the image is acquired when one holds the potential wells stationary by stopping the voltage clocks for some period of time (the "integration time") and then rapidly reads out the information by starting the clocks. Such a simple charge-coupled device should be practical only in special applications that allow very long integration times. The reason for this limitation is the "smearing" of the image that results when the shift register is clocked at the same time that it is illuminated.

A really practical charge-coupled linear image sensor is more complex. It consists of a photosensor array for accumulating the photocharge pattern plus an associated charge-coupled shift register with one charge-coupled element for each photosensor element in order to move the resulting charge packets to an output point. The elements of the photosensor array are individual charge-coupled storage elements with a common electrode called a photogate. They are electrically separated from one another by a highly concentrated *p*-type region called a channel stop. The photosensor array is separated from the charge-coupled shift register by a region over which there is an electrode called the transfer gate.

In operation the photogate voltage is held high and the charge generated by the incident radiation (the photocharge) is collected by the individual photosensor elements. At the end of the integration time the transfer-gate voltage is raised from its normally low voltage condition. The charge-coupled shift-register electrodes adjacent to the photosensor elements are also brought to a high-voltage state. The photogate voltage is then lowered and the accumulated photocharge transfers to the shift register. After that is accomplished the transfer-gate voltage is lowered and the photogate voltage is brought back to its normally high state for another integration period. Meanwhile the charge-coupled shift register is clocked for the purpose of reading out the charge pattern.

A high-density image sensor is more economically designed with one shift register on each side of the photosensor array. Since there must be one charge-coupled element for each photosensor element, the distance between photosensor elements is equal to the distance between the shift-register electrodes for a two-phase charge-coupled shift register and is equal to 1.5 times the distance between shift-register electrodes for a three-phase charge-coupled shift register. In this example the signal charge from the two three-phase shift registers is transported to a three-phase, two-element register for delivery to the on-chip preamplifier. If two-phase technology is used, however, it is possible to shift the charge directly into an output diode, which is in turn the input to the on-chip preamplifier. Note that in either case the information-output rate of the device is twice the rate of either of the long shift registers. It is clear from this example that a two-phase charge-coupled structure not only is easier to clock but also is more economical to lay out for a practical device. Even though it is somewhat more difficult to manufacture because of the required asymmetry, it is likely to dominate future designs of charge-coupled devices when fully developed.

A linear image sensor can be made to produce conventional two-dimensional images [*see illustration on next page*].



RELATIVE SPECTRAL RESPONSES of a charge-coupled silicon photosensor element (*colored curve*) and the human eye (*black curve*) are compared. The semiconductor material absorbs not only visible light (.4 to .7 micron) but also near-infrared radiation (.7 micron to 1.1 microns). The absorption of such radiation by a silicon substrate results in the generation of electrons in a quantity proportional to the amount of incident radiation. It is this "electro-optic" property that enables charge-coupled devices to be used as image sensors.

The image to be sensed is placed on a rotating drum, which provides the necessary motion of the image with respect to the device. The speed of rotation is synchronized with the vertical scan of the monitor. The charge-coupled linear image sensor provides each horizontal video line for the monitor by a complete sensing and readout operation repeated rapidly to supply all the horizontal lines for a full frame. In many applications the device is the moving element in the system, as in aerial reconnaissance, where the device is located in an airplane or a satellite.

The quality of image reproduction achievable with a linear charge-coupled sensor is excellent, reflecting the large dynamic range of the image sensor [*see illustration on page 31*]. The dynamic range is the ratio of the maximum to the minimum detectable image intensity. The quality of the reproduction demonstrates the very high transfer efficiencies and low electrical noise levels that can be achieved in existing charge-coupled devices.

Area image sensors are useful primarily for television-type camera applications. The image is obtained by conventional line-by-line scanning of the array mosaic and reproduction of the resulting video signal on a standard raster-scanned cathode-ray-tube monitor. A charge-coupled area image sensor designed for such a readout mode can be designed in a manner analogous to the linear image sensor. As in standard broadcast television, the image is read out in two separate fields by first reading all the even-numbered photosensor elements in each column and then all the odd-numbered photosensor elements in each column rather than by reading the odd and even elements in parallel, as in the case of the linear image sensor.

The area image sensor operates as follows. Light falling continuously on the photosensor sites produces electrons, which accumulate as charge packets in the potential wells created by the photogate voltage. After an interval of a thirtieth of a second the charge packets collected in the photosensors adjacent to all the phase-1 electrodes are transferred to the region under the phase-1 electrodes by raising the phase-1 voltage and lowering the photogate voltage. The charge packets in photosensor sites adjacent to the phase-2 electrodes do not transfer because the phase-2 voltage remains low. After the phase-1 transfer takes place the photogate voltage again goes to its normally high state and more electrons begin to accumulate in the depleted photosensor sites. The charge packets in the opaqued shift register are now transferred to the horizontal shift register at the top of the array. Each vertical transfer fills the horizontal register, which is then read out completely, producing a line of video information at the output. After all these lines are read out (a procedure that takes only a sixtieth of a second) the photosensors adjacent to all the phase-2 electrodes are read out, and in a similar manner this second field is delivered as a video signal at the output. Finally, the entire operation begins again and is completed at regular intervals of a thirtieth of a second.

A typical image sensor designed to operate in this fashion consists of a rectangular 100-by-100 photosensor grid [*see illustration on page 22*]. Each photosensor element and associated readout electrode occupies only 1.9 square mils. All 10,000 elements fit on a chip that measures .12 by .16 inch. An image taken with a camera system using such a device can be displayed on a television monitor.

This image-sensing device and others made by charge-coupled techniques are still somewhat primitive, but they clearly point the way toward a powerful camera technology. The combination of solid-state reliability, low-voltage operation, low power dissipation, large dynamic range, metric reproducibility and visible and near-infrared response offers to the potential user a compelling advantage over vacuum-tube image sensors and other solid-state image sensors.

The charge-coupling concept is basically one of semiconductor electronics rather than one of electro-optics. Because of the electro-optic characteristics of silicon, however, the light-sensing properties of charge-coupled arrays have tended to dominate this new technology. Nonetheless, the data-handling properties of such arrays may be of equal or even greater significance.

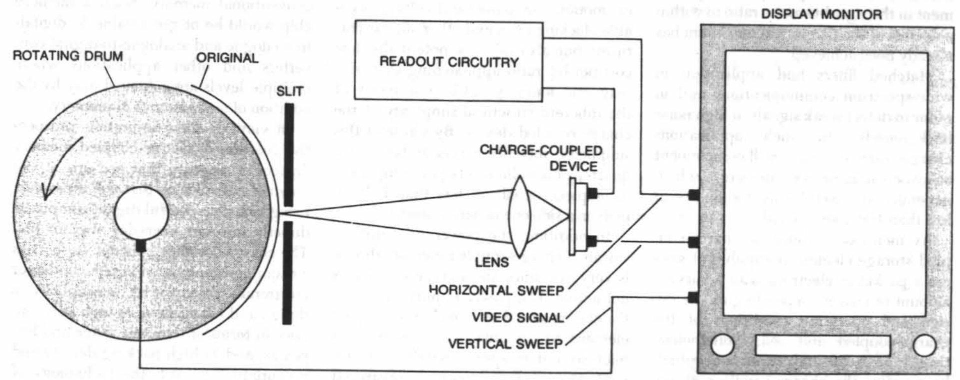
A charge-coupled semiconductor array is virtually ideal as a time-sampled analogue shift register. From the viewpoint of the electrical engineer this means a delay line where the delay is proportional to the readin/readout rate; if the array is long enough to contain the complete message, the readin and readout rates can be different and the maximum delay available is limited only by the thermal generation of random electrons. At low temperatures several minutes of delay are possible.

As a memory or digital-storage device, charge-coupled arrays can perform the functions of sequential access or hybrid tasks such as drum or disk storage. The use of solid-state charge-coupled arrays to eliminate all mechanical motion and parts is a strong advantage of a memory consisting of charge-coupled devices.

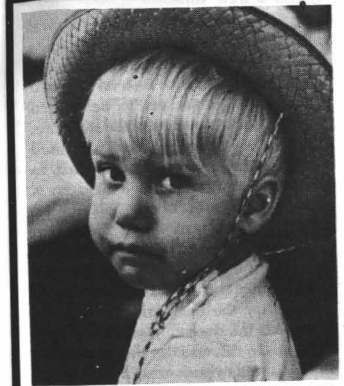
The intrinsic analogue nature of the charge packet in a charge-coupled device suggests broad potential for application to sampled-signal processing. In a fundamental sense the use of charge-coupled devices as image sensors is merely a special application of the device as an analogue shift register. If one restricts the definition of sampled-signal devices to those with an electrical (rather than an optical) input, then the predominant members of this class are variable delay lines and filters.

A delay line is a circuit that reproduces as accurately as possible an input signal delayed by a finite period of time. A delay line is "variable" if the time delay can be altered electrically. The charge-coupled device acts as a natural delay line since any signal placed on its input diode will appear at its output in sampled form after the interval required for the charge packets to be shifted through all the elements of the structure. The charge-coupled device can be used as a delay line in several ways. First, in the simple continuous mode the delay is equal to the number of unit cells divided by the frequency at which the device is clocked. Alternatively, whenever data appear in bursts, the charge-coupled shift register can be loaded with these data during the burst and the data retained for the desired interval and then read out. In this way the charge-coupled device is said to perform a "buffer" function.

A charge-coupled delay line offers major advantages over the more conventional glass delay line and even significant advantages over the more exotic acoustic-surface-wave devices [see "Acoustic Surface Waves," by Gordon S. Kino and John Shaw; Scientific American, October, 1972]. Among these are wide dynamic range (better than 60 decibels after 30 milliseconds at room temperature) and separate electronic control of propagation velocity and delay time. Delay lines with such flexibility will be of great value in communications and television applications and will simplify existing methods of producing controlled signal delays. One special application of significant interest is a "scan-rate converter" often required in video communications. Here the charge-coupled device operates in the buffer mode described above to accept and then read



TWO-DIMENSIONAL IMAGES can be reproduced with the aid of a linear charge-coupled image sensor in a variety of ways, one of which is outlined in this schematic diagram. The image to be sensed is placed on a rotating drum (*left*) whose speed of rotation is synchronized with the vertical scan of a conventional television display monitor (*right*). The charge-coupled device and the associated readout circuitry produce horizontal video lines at a rate rapid enough to build up a full-frame image on the screen of the monitor.



EXCELLENT REPRODUCTION obtained with a 500-element linear charge-coupled image sensor under widely varying light conditions is evident in these photographs. An apparatus similar to the one in the illustration on the opposite page was employed to scan the image. The photograph at left shows the original image to be scanned. The photograph at center shows the video display obtained from the charge-coupled system under optimum lighting conditions (30 foot-candles of illumination). The photograph at right shows the video display obtained from the same system but with the light level reduced 1,000 times; to produce this picture the charge-coupled device had to move packets of approximately 400 electrons each through a centimeter of silicon without dispersion.

out video frames at different rates so as to match practical transmission-system bandwidths with standard television-display requirements.

Extension of the simple delay-line concept leads to other sampled-signal processing devices. If a delay line is fabricated with interim taps at which the signal can be sensed and fed back to earlier stages in such a way as to affect the transmission of the data, then this structure can be used as a filter. Such a structure can be conveniently configured as a band-pass filter where the resonant frequency of the circuit is a direct function of the clock frequency. An improvement in the signal-to-noise ratio to within a decibel of the theoretical maximum has already been achieved.

Matched filters find application in wide-spectrum communications and in radar to detect weak signals in high noise backgrounds. In such applications charge-coupled devices will complement acoustic-surface-wave devices, which generally are useful only for delays of less than 100 microseconds.

As mentioned above, a charge-coupled storage element is capable of storing a packet of electrons with a varying amount of charge, depending on the design and operating conditions of the charge-coupled unit cell. Nonetheless, there is no reason one cannot conceptually quantize the charge-handling ability of the cell and view the device as a binary digital element. For example, one can arbitrarily say that if a storage element contains a charge less than half the saturation charge, it contains a "zero," whereas if it possesses a charge greater than half the saturation charge, it contains a "one." In this way the storage element becomes a memory "bit" and a charge-coupled delay line can be made to serve the function of a digital shift register or serially accessible memory. Since this function can be performed by other technologies also, one must ask what charge-coupling has to offer. The answer is cost-effectiveness. A charge-coupled memory not only has all the advantages of a conventional semiconductor component (compatibility with other electronic circuit elements, no mechanical motion, low power and voltage, variable clocking rates and other similar features) but also offers a potentially low cost-per-bit ratio approaching that of a magnetic memory. This is a result of the inherent structural simplicity of the charge-coupled device. By virtue of this simplicity, memory arrays as large as a quarter of a million bits per component on a piece of silicon less than half an inch on a side can be envisioned.

In addition, the power necessary to sustain a charge-coupled memory device is very low since the storage element is not active. The power required to move the charge stored on one charge-coupled element to an adjacent element in a microsecond is approximately a microwatt. Moreover, in a properly organized memory it is not necessary to have all bits moving simultaneously. Thus a one-megahertz, one-megabit charge-coupled memory device would require a power of somewhere between a milliwatt and a watt to sustain it, excluding logic and other functions. The volume required for such a memory is less than that of a pack of cigarettes.

Another advantage lies in the fact that the charge-coupled device is basically analogue in nature. It is thus possible to store more than one data bit in each memory cell. This can be done by storing any one of a number of discrete levels of charge in each cell, thereby greatly increasing the information-packing density. For example, a 100,000-cell device capable of handling eight levels of charge is comparable to a 300,000-bit conventional memory. Such a memory chip would be of great value in digital-to-analogue and analogue-to-digital converters and other applications where multiple levels are achieved only by the addition of vast amounts of memory.

In view of these important prospective features of charge-coupled memory devices it appears that we are at the dawn of a revolution that will ultimately bring today's powerful digital computers directly into our everyday way of life. The charge-coupling concept, in short, is a major new innovation in semiconductor electronics. By virtue of its simplicity in design and fabrication, its high performance in terms of dynamic range and low power, and its high packing density and potentially low cost, the technology of charge-coupling will create major and unique new applications for semiconductors that will have a direct impact on our lives.

Performance characteristics of a producible NTSC - compatible charge-coupled device (CCD) image sensor

Abstract

Brief reviews of the structure and normal operating conditions for manufactured versions of 488 by 380 element CCD image sensors are followed by descriptions of the performance available from typical devices and by description of common types of cosmetic blemishes which limit the yield of production sensors.

The 488 by 380 element sensors are fabricated by buried channel CCD technology. They utilize an inter-line transfer technique to achieve a high CTF at Nyquist frequencies, which results in crisp imagery from reasonable die areas. The sensors also offer wide dynamic range, good low light level capability, and compatibility with NTSC quality requirements.

Introduction

The basic concepts for a television-compatible inter-line-transfer CCD image sensor were developed in 1972. The first working samples of NTSC-compatible 488 by 380 element buried channel CCD image sensor arrays were demonstrated in 1975. These initial experimental sample arrays provided convincing evidence of the superior technical performance made available by the inter-line-transfer device organization, and also provided proof that significant improvements in silicon material and fabrication technology were required before the complex large-area monolithic image sensors could be produced in volume.

Production of 488 by 380 element sensors today still requires careful and skillful engineering control of fabrication procedures, but the technological advances which have been made permit 488 by 380 element sensors to be manufactured on an upward ramping production schedule with predictable yields to increasingly tighter device performance specifications.

This paper, in order to illustrate the substantial progress made to date in the areas of image sensor manufacturing and development engineering, reviews the performance features and limitations of recently-produced image sensors. The performance review is preceded by an outline description of the 488 by 380 element sensor structure and by an outline of the required sensor operating controls and signals.

Device structures

The 488 by 380 element charge coupled area imaging device (CCAID488) has die dimensions of 397 by 475 mils (Fig. 1). There are twenty-five potentially good die, plus one process test die of equal size, on a three inch wafer.

A CCAID488 (Fig. 1) is a self-scanned monolithic improved-performance replacement for a vidicon camera tube suitable for low-light-level, low power consumption video camera systems. The sensor produces an output which can be compatible with the NTSC quality standard for black and white television broadcasting (Fig. 2). The precise location of each photosite within the sensor allows accurate identification of image components for ease in signal processing and for image measurements which are free of geometric distortion.

The active area of the image sensor (Fig. 3) contains a matrix array of 185,440 photosites arranged into 488 lines and 380 columns. The overall dimensions of the active image sensing area are 8.8 by 11.4 mm, which has an image diagonal measurement of 14.4 mm.

The sensor contains 380 buried channel CCD shift registers which are used for vertical transport of photosite-accumulated image data, and one horizontal shift register for transport of image data to the charge-sensing video output amplifier. Both horizontal and vertical registers are controlled by external two-phase clock signals.

A photogate electrode controls transfer of data from the photosites into the vertical shift registers. The polarity of the vertical clock signals when the potential of the photogate lead is lowered determines whether the even-numbered or odd-numbered lines of photosite data are transferred to the vertical registers at the start of each field. The conventional operating mode of the 488 sensor results in a two-field-per-frame interlaced line video data output. Simple clock signal timing changes can be made externally to achieve a 244 line non-interlaced data output.

Electron charge packets are transported sequentially past the floating gate electrode of the video output amplifier (Fig. 4) by the horizontal register. The floating gate potential changes linearly with the quantity of charge resident in each packet. A pair of auxiliary gate electrodes aid in adjustment of the absolute potential of the floating gate.

The amplified and inverted video signal is sampled and held by a switching transistor and the gate node capacitance of the output source follower. The video output waveform is continuous, and includes a minimized sample clock energy content in the frequency band of interest.

The sensor includes a set of column antiblooming sink diodes at the top of the vertical shift registers which suppress horizontal blooming when the array is illuminated past saturation.

Individual photosites (Fig. 5) are 12 by 18 μm rectangles which are positioned on 30 μm horizontal center-to-center spacings and 18 μm vertical center-to-center spacings. Photosites are separated horizontally by the vertical shift registers which are shielded from light by opaque metal stripes. The photosites are effectively contiguous along the vertical axis, since photon absorption is unhindered by the barrier region which provides vertical site separation.

Portions of each photosite are covered by 1, 2, or 3 layers of near-transparent polysilicon gate electrode material, and by various layers of dielectric which insulate the gate electrodes.

Sensor operation

The 488 image sensor requires a single V_{DD} supply voltage of +12-15V for proper operation. A current of about 3.5 mA is used by the output amplifier. The antiblooming structure requires a dc voltage of about 10V. A dc source which can be adjusted over a range of 5-10V, at a current level of less than 1 μA, is needed to bias the source of the floating gate stage of the output sense amplifier. Sensor internal dc power consumption is about 50 mW.

Seven clock signal inputs provide timing control to the CCD shift registers, the photogate electrode, and the sample and hold output amplifier of the CCAID488. Figure 6 shows a timing signal sequence which is scaled for sensor operation at standard television scanning rates (30 frames per second, 2 fields per frame). There are no stringent requirements for relative clock signal timing, waveform overlaps, or rise and fall times.

Production CCAID488 sensors will provide satisfactory performance for most applications when all clock inputs except the two vertical transport signals swing from 0V (V_{SS}) to +5V. The two vertical transport clock swings are typically 0 to +9V. Clock swings below V_{SS} are seldom used.

The horizontal transport lines have capacitive loads of about 250 pf each. The horizontal clock frequencies for TV scan rates are 7.16 MHz. (The video data rate is equal to the horizontal clock frequency.) Higher capacitive loads are presented by the vertical transport and photogate clock input terminals but no difficulty is encountered in driving these leads because of the slow clock frequencies involved.

Data rates to above 14 M pixels per second (60 frames per second) are practical. The lower limit on the data rate can be extended to give frame periods of several tens of minutes if the sensor is cooled to reduce integrated dark signal nonuniformities to an acceptable amplitude.

A variety of hardware logic, PROM, and microprocessor timing control circuits have been developed to generate the sequence of timing signals which were shown in Fig. 6.

Sensor performance

Included among the well-known salient performance features of good CCAID488 image sensors are:

o Solid-state construction
o Low power consumption
o NTSC resolution capability (488 lines/frame, 380 pixels/line)
o Wide dynamic range
o Low light level capability
o Sample & hold video output

The continuous sampled and held video waveform at the sensor output can be used directly for many sensor applications. The waveform contains a short-duration sampling clock pulse which has very low energy content at the Nyquist frequency of the sensor, and the waveform can be satisfactorily cleaned up by simple low pass filtering.

The saturation-level video output signal level from the floating gate input two stage video sense amplifier at the output part of the image sensor is typically 1Vp-p, as shown. The saturation charge level is about 300,000 electrons. Shot noise content of the signal charge packets is equal to the square root of the signal; thus the signal to shot-noise ratio near saturation is about 54 db. At very low signal levels, the signal to temporal noise ratio is determined primarily by noise originating in the output sense amplifier which is about 100 electrons RMS at 25°C. In practice, the low light level performance is more often limited by thermally generated dark current nonuniformities than it is by temporal noise.

The buried channel fabrication technology results in excellent charge transfer efficiency, typically >.9999 per transfer, which prevents mixing of charge packets with subsequent loss of image sensor resolution. Figure 7 gives measured CTF responses for a sensor, plotted against the spatial image frequency normalized to the 30 μm horizontal and 18 μm vertical center-to-center spacings of array photosites. An 80% CTF at 380 TV lines per picture width is obtained because the photosites are separated horizontally by the opaque stripes covering the vertical shift registers. The register shields also prevent any smearing of the image vertically which would be caused by collection of image data in the register cells.

Demonstrations of good vertical and horizontal CTF response is evident in the resolution test chart photo (Fig. 8).

The spectral responsitivity of the sensor is a typical silicon detector curve, (Fig. 9) modified in the short wave length portions of the spectrum by photon absorption in the polysilicon layers which cover portions of the photosites, and by interfering and reinforcing reflections in the dielectric layers which separate the polygate structure layers. The quantum efficiency lines on Fig. 9 are valid for localized photosite response. (The Quantum Efficiencies shown on the graph are valid for light incident onto the photosites. For overall response, the numbers should be divided by 2-1/2 because the vertical register light shields cover about 60% of the sensor surface.)

Thermally generated carriers accumulate in the photosites and shift register cells and add directly to photon-generated carriers to form the charge packets sensed to generate the video output signal. A typical device, at 25°C and 33 MS integration time, will have a background dark signal (VBDS) of 1% of the saturation output level plus a dark signal nonuniformity (DSNU) signal caused by spatial inequality in leakage current over the sensor area. The V_{BDS} signal has no appreciable effect upon the appearance of a sensed image; the V_{BDS} charge adds negligible shot noise to the video. Dark signal nonuniformity is a serious limitation on sensor performance, especially when spatially regular DSNU structure is present. Current commercially-sold 488 sensors have a maximum specification for DSNU of 10% of Vsat at TV scan rates and room temperature ambient, typical commercial sensors exhibit a DSNU of less than 5% of Vsat.

Both VBDS and DSNU decrease exponentially with reduced chip temperature. Excellent sensor performance for most applications is achieved when the chip temperature can be reduced to 10°C or lower.

Photo lithographic irregularities can create spatial variation in photosite areas which can cause the photo-response to be nonuniform. Errors of this type occur, typically, at near-Nyquist spatial frequencies and usually have an amplitude considerably smaller than 5% of Vsat.

Photo response nonuniformities can also arise from spatial variability in carrier lifetime in the 1 square CM of active sensor area when the sensor image contains significant near infra-red spectral content. It is recommended that the sensor be used with an infrared reject filter for those applications where near IR response is not essential; the IR filter also preserves sensor resolution which can be degraded by the deep absorption level of IR photons.

Blemishes

The CCAID488 is a densely-packed monolithic chip which is 1 square CM in area. The large area, dense packing factor, device sensitivity, and the usual sensor application for presentation of visual images on a CRT display force the device into use as a vehicle for study of various microscopic and macroscopic effects which limit the performance available from all types of VLSI integrated circuits.

Blemishes which degrade sensor performance can exist or be induced into starting material wafers, or they can be introduced by processing "errors" which damage the several layers of dielectric and conductive layers which are built up on the sensor surface. The cosmetic effects of blemishes can be divided into area, single point, and linear defects.

Swirl patterns (Fig. 10) are a type of potential area blemish-inducing structure which exist in wafers before processing begins. The swirl patterns are generally believed to be nonuniform spatial patterns of impurity inclusions which are incorporated into crystals during growth of the silicon ingots. A small fraction of otherwise useful CCAID488 die are presently rejected at test because of excessive-amplitude DSNU shading caused by swirl. Swirl amplitude decreases exponentially with chip temperature, which permits swirl-blemished CCAID sensors to be used in many applications.

White clouds (Fig. 11) are localized areas which exhibit average dark currents appreciably higher than the background level. White clouds are also believed to be due to localized concentrations of donor impurities in the starting material. White clouds have a characteristically grainy appearance because they exhibit a large pixel-to-pixel dark current nonuniformity. White clouds are temperature sensitive, decreasing in amplitude by 50% for each 7-8 degree reduction in chip temperature.

Swiss cheese (Fig. 12) is a DSNU structural pattern which is attributed to variations in annealing effects in CCAID488 die. Process improvements have reduced the incidence of Swiss Cheese DSNU patterns outside of shading specification limits substantially in recent production lots. Swiss cheese also decreases exponentially with chip temperature.

Single point blemishes (SPBs) by definition are areas not larger than 3 contiguous pixels along any axis which exhibit a spurious response of 25% or more of Vsat at 25°C. Most SPBs affect a single pixel, about 20% of the SPBs affect 2 adjacent pixels. They originate from microscopic sources of thermal electrons which accumulate in individual photosites. More than 90% of the SPBs are exponentially reduced in amplitude by reduced chip temperature. Some SPB generation centers are believed to exist in wafer starting material, the majority are introduced during wafer fabrication. Current sensor manufacturing yields die with 2-200 SPBs per array; a typical die would have about 20 SPBs. A random sampling of SPBs can be seen in Figures 10, 11 and 12.

The most common type of column blemish found in the ILT type of device are black trails (Fig. 13). These blemishes are caused by "leaks" in the barrier walls which separate photosites from each other, photosites from the vertical shift register, and within the register itself. Some trails are of fixed length, others tend to shorten at increasing light levels. Some trails are preceded by a white column, some have white heads at their top. Register barrier trails replicate, i.e. they cause all data in the column below the black portion of the trail to move upward.

The most common means of creating a line (horizontal) oriented blemish in the CCAID488 is a short between the two vertical clock lines because of a dielectric defect. Devices exhibiting this type of defect are rejected by dc die testing, hence line oriented defects are seldom seen in packaged sensors.

The large die area and densely packed complex structure of the CCAID488 provides an enormous number of opportunities for process errors or structural damage which can create blemishes degrading the cosmetic performance of a sensor. In spite of these opportunities, it is now well-established that near-perfect sensor die can be produced on a regular basis by careful wafer fabrication procedures.

Sensors which have limited blemish content can be used for many applications, also. Some uses for the sensor need good performance only in selected sensor areas, some users can ignore or suppress black trails and limited numbers of single point blemishes. Cooling of sensors which have dark signal nonuniformity patterns exceeding tolerable levels in particular application is very practical, as is storage and subtraction of DSNU and PRNU blemishes in many systems.

Summary

A 488 by 380 element buried channel CCD image sensor is now being reproducibly manufactured. The inter-line transfer structure used for the sensor provides broadcast quality resolution in a 397 by 475 mil die. The sensor has a dynamic range of 1000:1, low light level capability, a wide range of scanning rates, and an internal power consumption of about 50mW. Precision optical measurement systems can use the sensor because it is geometrically precise and because sensor readout is controlled by digital clock signals. The video output signal of the sensor is a sampled and held waveform for ease of use.

Dramatic improvements have been made in the cosmetic quality level of the 488 by 380 element sensors, as can be seen in Figures 14 and 15. Fabrication process development and sustaining engineering work is continuing in order to achieve higher yields of die with lower blemish counts. The present sensor design has been firmly shown to be viable, and it is anticipated that the CCAID488 will continue to be commercially available in various cosmetic quality grades.

Acknowledgments

The improvements in processing technologies which have allowed the 488 by 380 element sensor to become manufacturable were accomplished by a skilled team working under the overall direction of W. Steffe, A. Watkins, and P. Radcliffe. Insight into causes of sensor blemishes has been provided by A. Tickle and O. Barrett. L. Meyers has performed many of the detailed measurements reported above. The continued insistence on performance quality of sensors by I. Hirschberg, Fairchild, Syosset, N. Y., has significantly aided the development efforts.

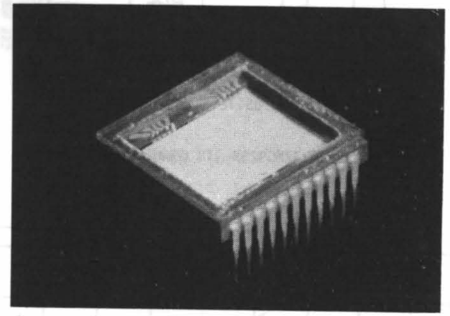


FIG. 1 THE NTSC-COMPATIBLE 488 BY 380 ELEMENT CCD IMAGE SENSOR

FIG. 2 MONITOR DISPLAY OF CCAID488 IMAGE

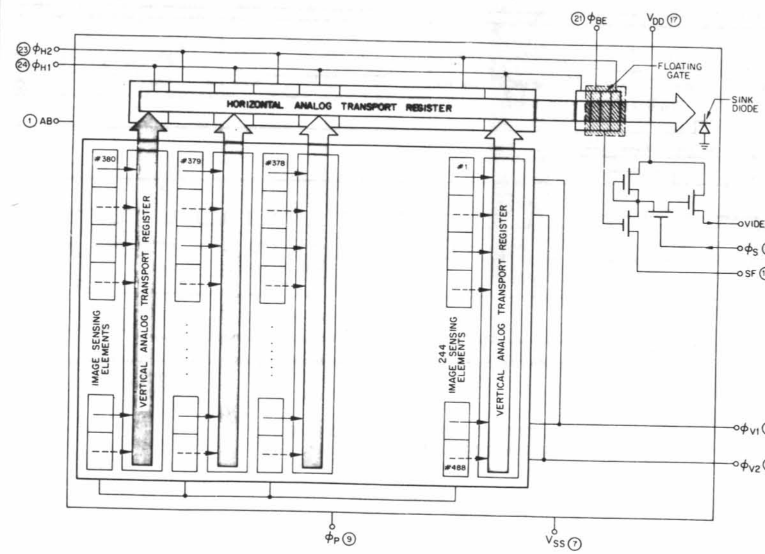


FIG. 3 CCAID488 BLOCK DIAGRAM

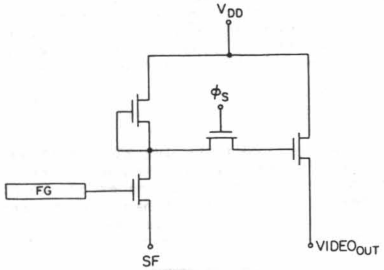


FIG. 4 CCAID VIDEO OUTPUT AMPLIFIER

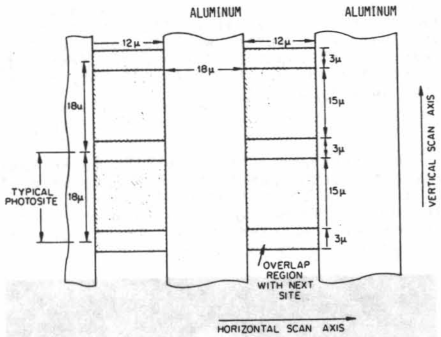


FIG. 5 CCAID PHOTOSITE STRUCTURE

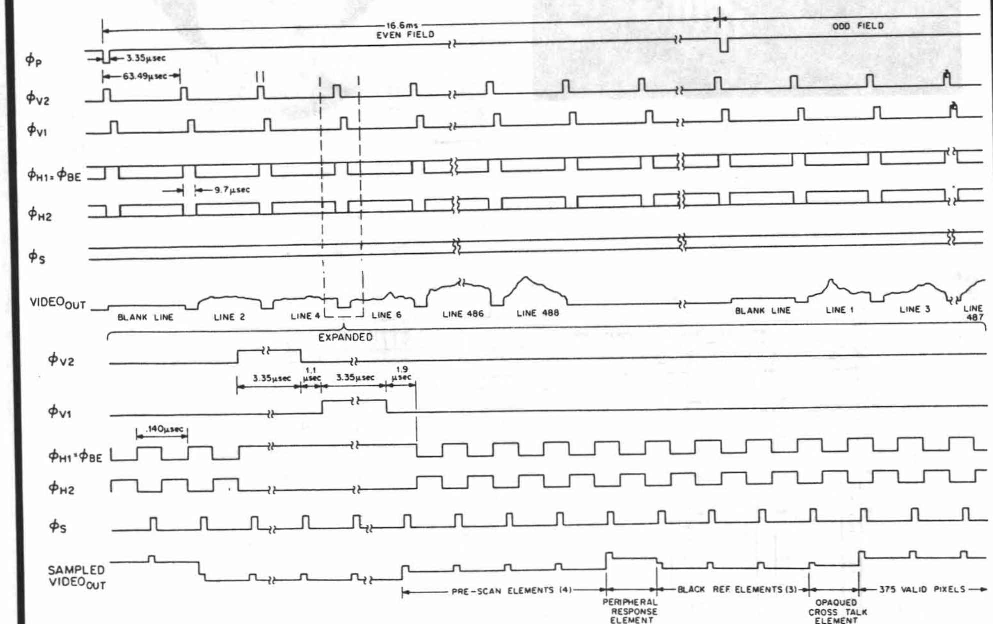


FIG. 6 TIMING DIAGRAM FOR OPERATION OF THE CCAID488 AT STANDARD TV RATES

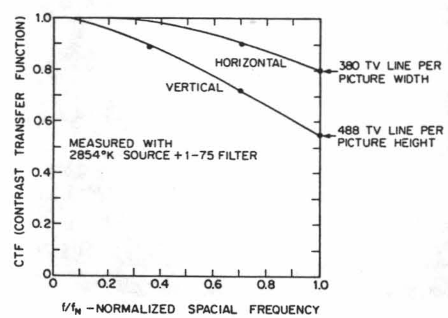


FIG. 7 MEASURED CTF RESPONSE OF CCAID488

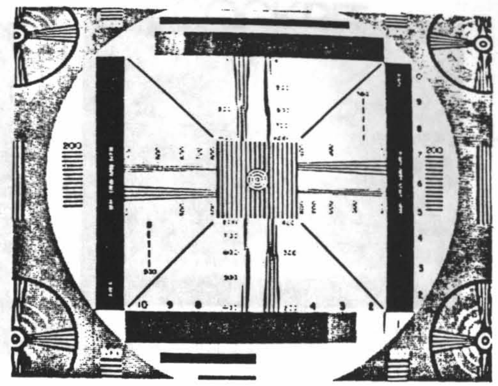


FIG. 8 MONITOR DISPLAY OF RTMA TEST PATTERN

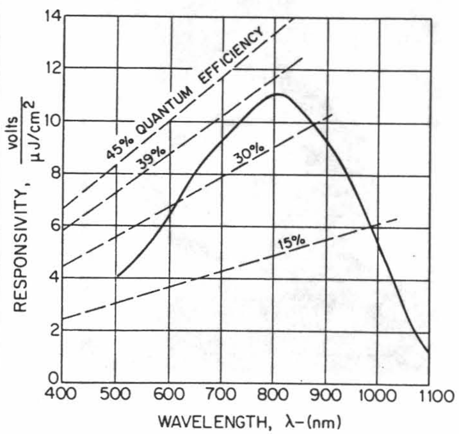


FIG. 9 CCAID488 SPECTRAL RESPONSE

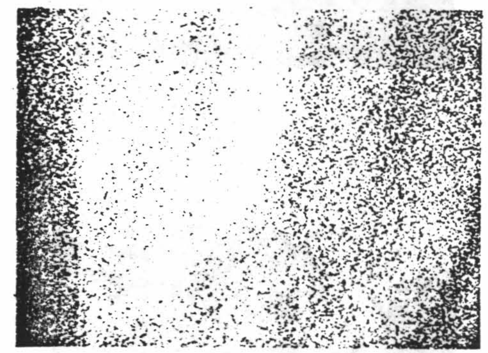


FIG. 10 SWIRL PATTERN, MONITOR PHOTOGRAPH TAKEN AT HIGH VIDEO GAIN SETTING

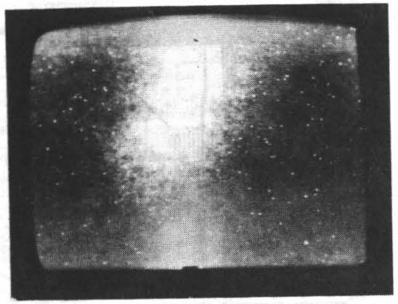


FIG. 11 A CCAID488 "WHITE CLOUD" BLEMISH

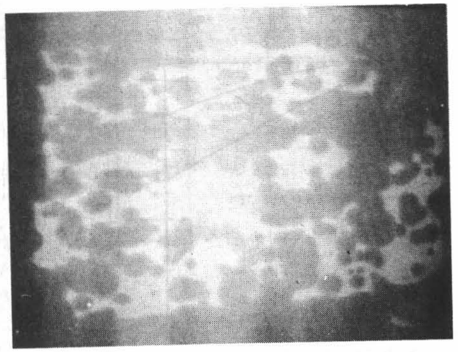


FIG. 12 "SWISS CHEESE" DARK CURRENT PATTERN IN A CCAID488

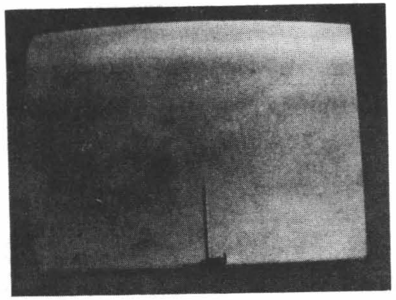


FIG. 13 "BLACK TRAIL" BLEMISH IN A CCAID488 UNDER UNIFORM ILLUMINATION

FIG. 14 MONITOR DISPLAY OF A CCAID488 DETECTED IMAGE

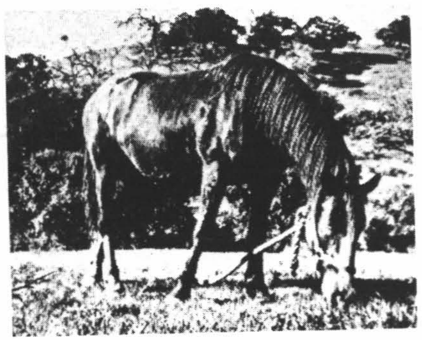


FIG. 15 MONITOR DISPLAY OF A CCAID488 DETECTED IMAGE

A SOLID STATE (CCD) COCKPIT TELEVISION SYSTEM

ABSTRACT

The Cockpit Television Sensor (CTVS) System provides a monochrome video tape record of aircraft displays and instruments, such as the Head Up Display (HUD) gunsight, radar display, etc., and in addition records cockpit audio data. When used with the HUD, the recording shows the outside world scene as viewed by the pilot together with the HUD symbols. Two displays, such as HUD and radar, can be simultaneously recorded on a single tape using a CTVS split-screen mode. This paper describes performance characteristics and capabilities of the system, which is centered around a small versatile highly reliable solid state Charge Coupled Device (CCD) TV camera, which has already been flight proven on the F16, F15, F14 and F4, and qualified to full military specification for flight equipment. (Appendix A provides tabulated summaries of environmental levels.)

The sensor head for the CTVS has a volume under 100 cubic centimeters, about the same volume as a cigarette pack, and includes an f/2.8 auto-iris lens having a 5,000 to 1 dynamic range, providing automatic hands-off dawn to dusk operation.

INTRODUCTION

Traditionally, tactical fighter aircraft have been equipped with film cameras to record gunsight/HUD images for both training and combat missions. The Cockpit Television Sensor (CTVS) system fulfills a similar function with the added feature of recording cockpit audio together with the video and offering the option of real time display in the rear cockpit. In addition, the use of an Airborne Video Cassette Tape Recorder (AVTR) extends the recording capability to 30 minutes, and the use of a split screen converter permits two video sources to be simultaneously recorded on the same video cassette, i.e., HUD and radar, or HUD and EO weapon display. For post-flight playback immediately after landing, a standard 3/4" U-matic video cassette tape machine and TV monitor are used. This same equipment is used for split screen playback, which requires no additional special purpose components. The reason for this is that "split screen" is recorded as a single EIA RS170 compatible frame, with only one half of the monitor display used for each camera recording, so that the two camera pictures appear side by side on the same screen. Each camera picture must be compressed horizontally, in order that both pictures can be viewed on a single screen. The use of slow motion, and stop-action, playback on the VTR permits side by side comparisons of the two images on a frame by frame basis with no additional special equipment.

SYSTEM DESCRIPTION

A simplified CTVS block diagram is shown in Figure 1 together with a photograph in Figure 2. The airborne system assemblies comprise the CCD television camera, the Airborne Video Cassette Tape Recorder (AVTR) and the AVTR Remote Control Unit. The TV camera is made up of two separable subassemblies. These are the Video Sensor Head (VSH) and the Electronics Unit (EU). The VSH contains the CCD sensor module, auto-iris lens and interface electronics, including line drivers, which allow the VSH to operate over a maximum of 7 meters of cabling to the EU. The EU assembly contains the clock generator, control logic, video processing, built-in-test (BIT) circuits, BIT switches and indicators and the power supply.

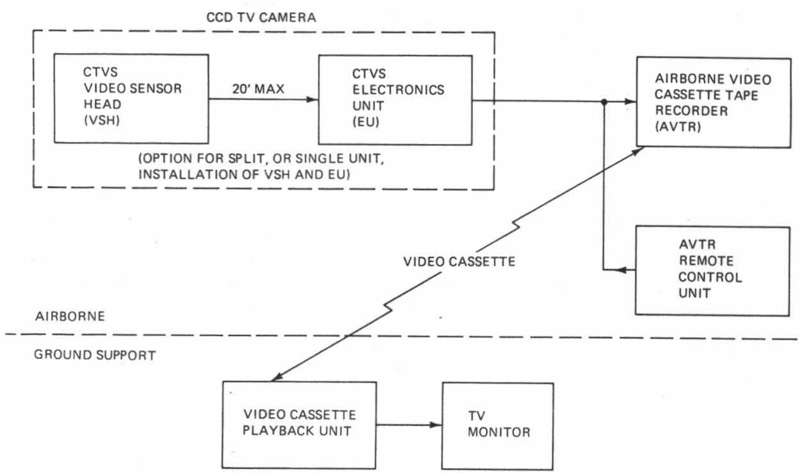


FIGURE 1. CTVS BLOCK DIAGRAM

In aircraft which have provision for the KB26 series of film gun cameras, the CTVS camera can be installed as a single assembly in the same location previously occupied by the KB26 camera. In these aircraft (such as the F16, A10, etc.) the VSH is plugged directly into the EU, and the complete camera is installed as a single assembly using the same configuration as the KB26. Figure 3 shows the CTVS camera in this mode, and Figure 2 shows the camera used as a split assembly together with the remaining components of the airborne system. The split mode of operation is used on aircraft such as the F15 and F14 where there is no existing provision for a HUD camera. In these cases, the small size of the VSH, (see Figure 6) makes it practical to mount it on the sun shield, directly in front of the HUD combining glass, with minimum obscuration of the pilots field-of-view. The maximum obscuration of 23mm due to the CCD sensor-lens, which is centrally located in the pilots field-of-view, has been demonstrated to have no impact on pilot performance.

The composite video output from the CTVS camera is wired directly to the AVTR input (see Figure 1) with a maximum cable length of 150 meters. In most installations, camera power comes on with aircraft power, and the camera is continuously operating during flight, eliminating the need for the addition of cockpit switches and indicators. This simplification is practical because of the demonstrated reliability of the camera. Video from the camera can be recorded by switching the AVTR control box switch from Stand-by to Record. The AVTR control box typically has a three position control switch. These positions are Power-Off, Stand-by and Record. In the Stand-by mode, the AVTR cassette is fully threaded or "loaded" and recording can be started instantaneously by closing the Record switch. In the Power-Off position, the cassette is unthreaded, as when installing or removing the cassette. It takes approximately five seconds to complete the tape threading cycle when going from Power-Off to Stand-by.

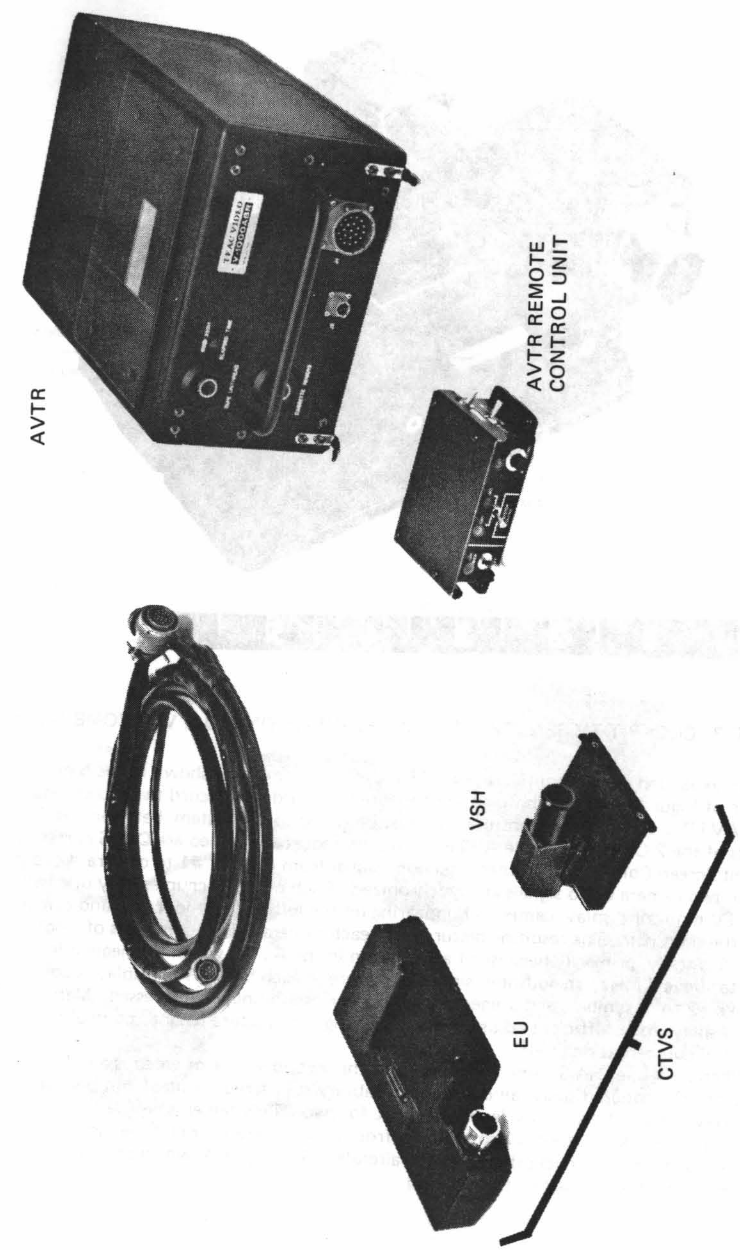


FIGURE 2. CTVS SYSTEM - CTVS CAMERA, AIRBORNE VIDEO CASSETTE TAPE RECORDER, AND AVTR CONTROL UNIT.

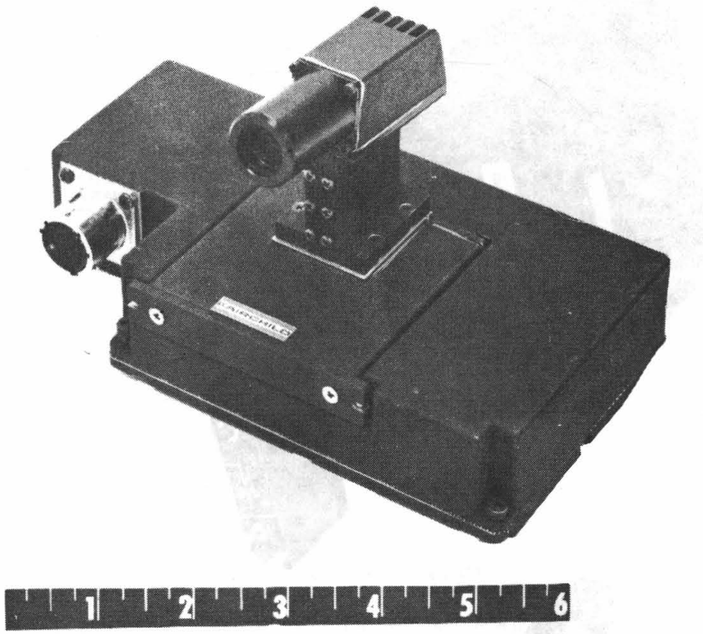


FIGURE 3. COCKPIT TV SENSOR – F16 CONFIGURATION (EU & VSH COMBINED)

An expanded system configuration which uses two cameras is shown in the block diagram of Figure 4 and the photograph of Figure 5. In order to record two video inputs to the AVTR, a Split Screen Control Unit must be added to the system, between the outputs of the 2 Cameras and the AVTR. If the two sources of video are CTVS cameras, the Split Screen Control Unit routes a gen-lock signal from camera #1 to camera #2 so that the two camera video signals are synchronized. Each picture occupies only one half of the TV monitor display, camera #1 appearing on the left half of the screen and camera #2 on the right half. The resulting picture from each camera suffers some loss of resolution horizontally, primarily because of attenuation in the AVTR which has negligible response above 4 MHz. In addition, since the picture in each half of the display is compressed by 2 to 1, symbols and scenes will appear correspondingly compressed. Many CCTV displays have sufficient adjustment range using the "picture height" control to permit full compensation.

When only one CTVS camera is in use, and the second source of video is a radar display or EO weapon display, an expanded capability split screen control unit permits similar recording and display as described above for two CTVS cameras.

A separate video output is also available from each camera for real time display on a monitor in the rear cockpit of two seat aircraft. (See Figure 4, which includes an airborne TV monitor as part of the system.)

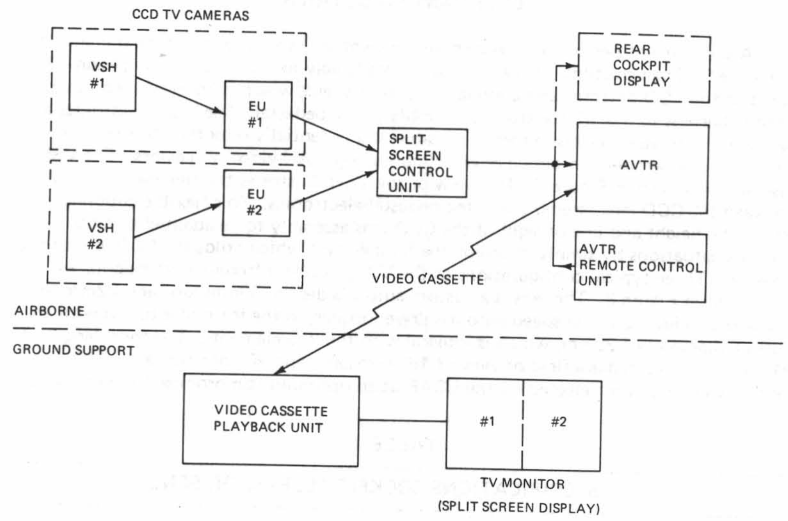


FIGURE 4. CTVS SPLIT SCREEN BLOCK DIAGRAM

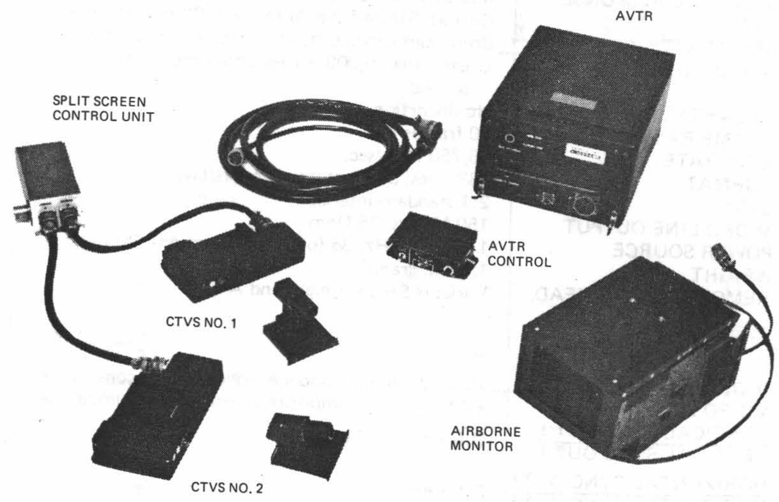


FIGURE 5. CTVS SYSTEM – SPLIT CONFIGURATION, INCLUDING AVTR AIRBORNE MONITOR AND SPLIT SCREEN CONTROL UNIT

CTVS CAMERA DETAILS

A summary of performance parameters is given in Table 1, and outline dimensions in Figure 6. The versatility of the camera resides largely in the unique VSH design. This contains the CCD detector and a miniature auto-iris lens, which is coupled via a flexible printed harness to a small electronics assembly in the pedestal. The VSH electronics are necessary to drive up to seven meters of cable to a potentially remotely located Electronics Unit assembly containing power supplies, logic and video processors. The VSH assembly is shown in Figure 7. This view of the VSH illustrates the flexible coupling between the CCD-lens assembly and the pedestal electronics. This flexible coupling allows the height and line of sight of the CCD-lens assembly to be adapted to most practical situations by simply changing the hollow stem which holds the CCD-lens to the pedestal. Three typical configurations of the VSH, having different stem heights, are illustrated in Figure 8. The lens is a custom auto-iris design, 30mm long and 22mm in diameter, including a high speed auto-iris drive torquer, in the form of a toroid with an outside diameter of 20mm, which is integral with the lens elements. The focal length of 31mm provides a camera field-of-view of 16° vertically and 20° horizontally. This field-of-view has been selected by the USAF as an optimum compromise for most HUD

TABLE 1

SPECIFICATIONS COCKPIT TELEVISION SENSOR	
GENERAL	
SENSOR	Fairchild CCD Array (488 lines X 380 pixels/line)
SPECTRAL RESPONSE	450 to 1060 nanometers (without filters)
LENS	Custom 31mm f/2.8 Auto-Iris ("C" mount option)
SENSITIVITY	Scene luminance 5 ft. Lamberts with S/N of 20 dB
ALC DYNAMIC RANGE	Greater than 5,000:1 (response time less than one second)
GEOMETRY	No distortion
FRAME RATE	30 frames/sec.
LINE RATE	15,750 lines/sec.
FORMAT	488 lines, 380 picture elements/line
SYNC	2:1 standard interlace
VIDEO LINE OUTPUT	150 Meters, 75 Ohm
POWER SOURCE	115V, 400 Hz, 3ϕ (or 28V DC option), 20 watts
WEIGHT	1.1 Kilograms
REMOTE SENSOR HEAD	Variable Sensor Height and Angle
OUTPUTS – INPUTS	
VIDEO 1	1V to 3V p-p, composite video (RS170 compatible)
VIDEO 2	1V to 3V p-p, composite video (RS170 compatible)
VERTICAL SYNC OUT / $\overline{\text{VERTICAL SYNC OUT}}$	Differential TTL
HORIZONTAL SYNC OUT / $\overline{\text{HORIZONTAL SYNC OUT}}$	Differential TTL
GEN-LOCK – INPUT	RS170 Comp. Sync 2V p-p
EVENT MARK – INPUT	28V DC (unregulated) ±4V DC
SPLIT SCREEN – INPUT	TTL Logic Low

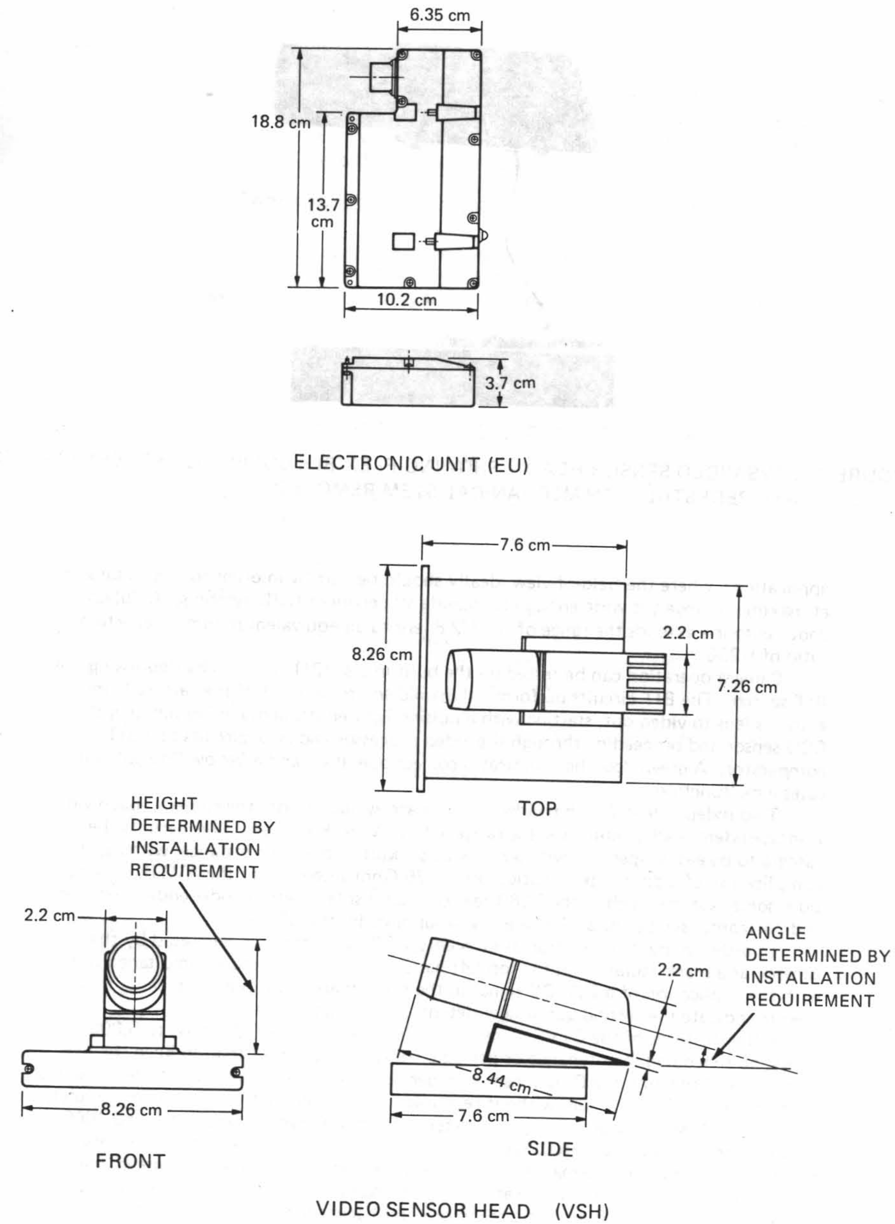


FIGURE 6. CTVS OUTLINE DIMENSIONS

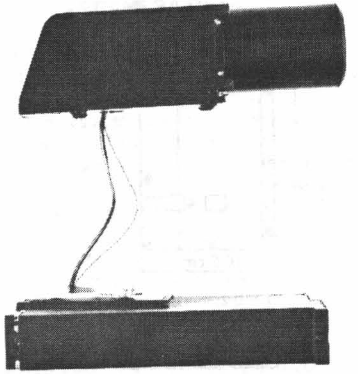


FIGURE 7. CTVS VIDEO SENSOR HEAD – SHOWING FLEXIBLE COUPLING BETWEEN CCD-LENS AND PEDESTAL WITH MECHANICAL STEM REMOVED

applications, where the field-of-view ideally should be narrow in order to record targets at maximum range yet wide enough to include all pertinent HUD symbols. A "black-spot" auto-iris extends the range of the f/2.8 lens to an equivalent minimum aperture ratio of f/256.

Camera operation can be tested by the built-in-test (BIT) circuits by depressing the BIT switch. The BIT circuits perform a dynamic end-to-end test of the camera from auto-iris lens to video out, starting with a pulsing light emitting diode illuminating the CCD sensor and proceeding through the video processor and sync circuits to a BIT comparator. A green "go" light indicates correct operation and a yellow "no-go" indicates a malfunction.

Two independent 75 Ohm video outputs are available from the camera. Each video is independently adjustable over the range 1V to 3V peak-to-peak. This permits the camera to be easily operated with a rear seat cockpit display, for instance, without the complication of a double termination on the 75 Ohm video line to the AVTR. In addition, some systems, such as the F16B rear cockpit display, require independent vertical and horizontal sync signals. These are also supplied by the CTVS.

In order to identify key frames or events, an "event mark" is generated by the camera, as a black rectangle in the top left hand corner of the picture, simultaneously with the application of a 28V DC signal to the event mark input pin. Typically, this is used to indicate the second gun trigger detent, or a weapon release.

Other features of the CTVS camera include a theoretical MTBF close to 5,000 hours, no scheduled maintenance or periodic adjustments, (other than to keep the lens clean!). Additionally, the CCD sensor is impervious to damage from sun, if the camera is pointed directly into the sun, without recourse to any special safety shutters or circuits.

The CCD sensor spectral response extends from 450 nanometers to beyond 1060 nanometers. However, for HUD recording applications, carefully selected filters are critical for optimum performance. This is because most HUD displays are green, with a narrow peak in the response curve at around 550 nanometers. Typically, the pilot can discern the HUD symbols against a much brighter background because of color discrimination. The monochrome CTVS camera, however, may not reproduce the scene with sufficient contrast for the HUD symbols to be visible, since the bright background may

wash out the relatively much lower intensity HUD. Therefore, in most HUD applications, a combination of infrared blocking and green pass filters is used. The result of the latter is that overall camera sensitivity is traded off for selectivity. Some HUD displays have both green and orange, or even red, symbols or reticles, and these cases must be treated individually. In all cases, the CTVS has provision for the addition of filters, and lens hood, which screw directly into the CTVS lens barrel.

AIRBORNE VIDEO–CASSETTE TAPE RECORDER

Table 2 provides a summary of key performance specifications of the AVTR, and Figure 9 shows the mechanical outline. The tape recorder uses the standard 3/4 inch U-Matic video-cassette, for easy loading and unloading in the aircraft. The maximum

TABLE 2

TEAC V-1000AB-R

AIRBORNE VIDEO–CASSETTE RECORDER
(Record Only)

SPECIFICATIONS

GENERAL	
Recording Systems	Rotary two-head helical scan system
Maximum Recording Time:	30 Minutes
Tape Format:	U-Matic "S" standard cassette (3/4 inch)
Power Source:	28V DC aircraft power (MIL-STD-704 B)
Power Consumption:	30 Watts
Dimensions:	15.2cm (h) X 33cm (d) X 24.4cm (w), excluding the handle.
Weight:	10.4 kilograms
VIDEO	
Signal System:	EIA b/w standard. (525 lines/frame, 60 fields/sec.)
Bandwidth:	3.5 MHz -4.0 dB when referenced to the response at 1 MHz.
S/N Ratio:	More than 40 dB
Resolution:	More than 340 lines
Linearity:	10 gray scales minimum
Input:	1V p-p +2.0, -0.5: 75 Ohms unbalanced. AGC.
Output:	E to E at 1.0V p-p, 75 Ohms.
AUDIO	
Number of channels:	2
Input:	0.5V p-p nominal, 0.1 to 10V p-p with AGC. Selectable input impedance.
Bandwidth:	80 Hz to 15,000 Hz ±3 dB
S/N Ratio:	More than 40 dB
Distortion:	Less than 2.5%
Event Mark:	1,000 Hz tone on audio track #1.

recording time is currently 30 minutes, with automatic rewind at the end of tape. Although longer running tapes are available from some manufactures, these are not yet recommended for airborne use.

The recorder can be mounted in any vertical axis, or horizontally, using shock isolator mounts, but installation upside down is not recommended.

In addition to the video recording, two independent audio channels are available for direct recording of cockpit audio, and for tone cuing such as for an event mark.

Typically, the AVTR Control Unit is switched to stand-by immediately prior to flight or shortly after take off. In this mode, the recording heads are rotating at full recording speed, and the video tape has been automatically loaded and wrapped around the recording head. This permits the AVTR to be instantaneously switched to the "Record" mode with no delay or start up time. However, it is not ideal to operate in this mode indefinitely, without recording, since the tape heads are in continuous contact with the tape and this can eventually lead to clogging up the recording head, or to tape damage, or both. When the AVTR control switch is turned to OFF, the tape cassette automatically unwinds from the capstan and recording head, and is then ready for manual removal at the end of flight. If aircraft power (28V DC) is removed prior to switching to the OFF position, the tape will remain loaded and it will not be possible to remove the cassette.

SPLIT SCREEN CONTROL UNIT

The split screen control unit is required where the video outputs from two cameras are to be simultaneously recorded on one video tape. Key specifications are given in Table 3. The control unit is designed so that either Camera #1 or Camera #2 can be selected and recorded normally, or both camera outputs can be combined, as described previously.

The simplest configuration for the split screen control unit is if both video sources are CTVS CCD cameras, since the latter have a built-in capability for split screen operation by application of a logic signal to the camera split screen control signal input pin, which is in the aircraft interface connector.

For systems where one signal source is a CTVS CCD camera and the second is another camera (EO weapon) or radar display, the split screen unit capability can be expanded to modify and process the second camera, provided that the video is in EIA RS170 format.

The full video (i.e., full camera field-of-view) of both cameras is recorded in all cases. This was found to be preferable to cropping portions of each image in order to combine them, in spite of the penalty of horizontal distortion, since in most cases valuable information is lost from cropping.

TABLE 3

SPLIT SCREEN CONTROL UNIT – SPECIFICATION SUMMARY	
Video Inputs:	Input 1 – CTVS Input 2 – Other RS170 Source
Video Output:	RS170 with left/right split, CTVS on left, RS170 source on right, reproduction 100% of both sources
Output Format Modes:	1. Left/right split 2. Input (CTVS) – Full Screen 3. Input 2 – Full Screen
Power:	115V, 400 Hz, 3 Phase or 28V DC
Size:	6.35cm X 7.6cm X 15.24cm
Weight:	Less than 1 Kilogram

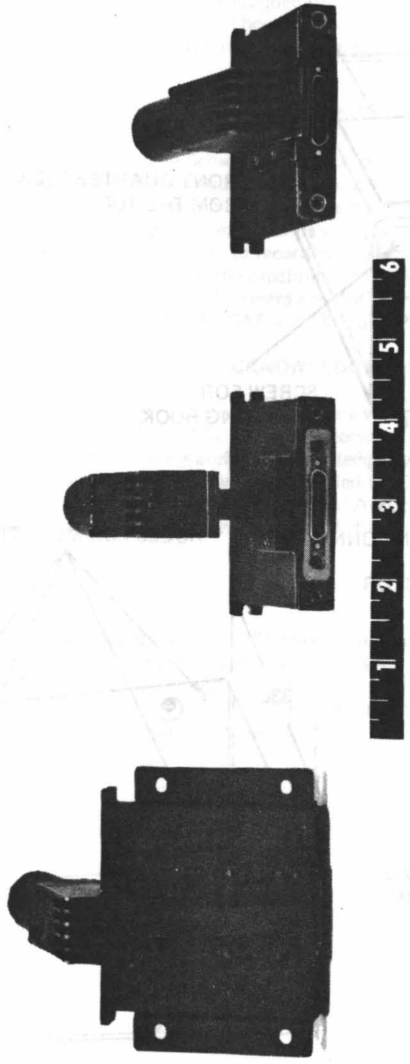


FIGURE 8. VIDEO SENSOR HEAD – ILLUSTRATING THREE TYPICAL STEM CONFIGURATIONS

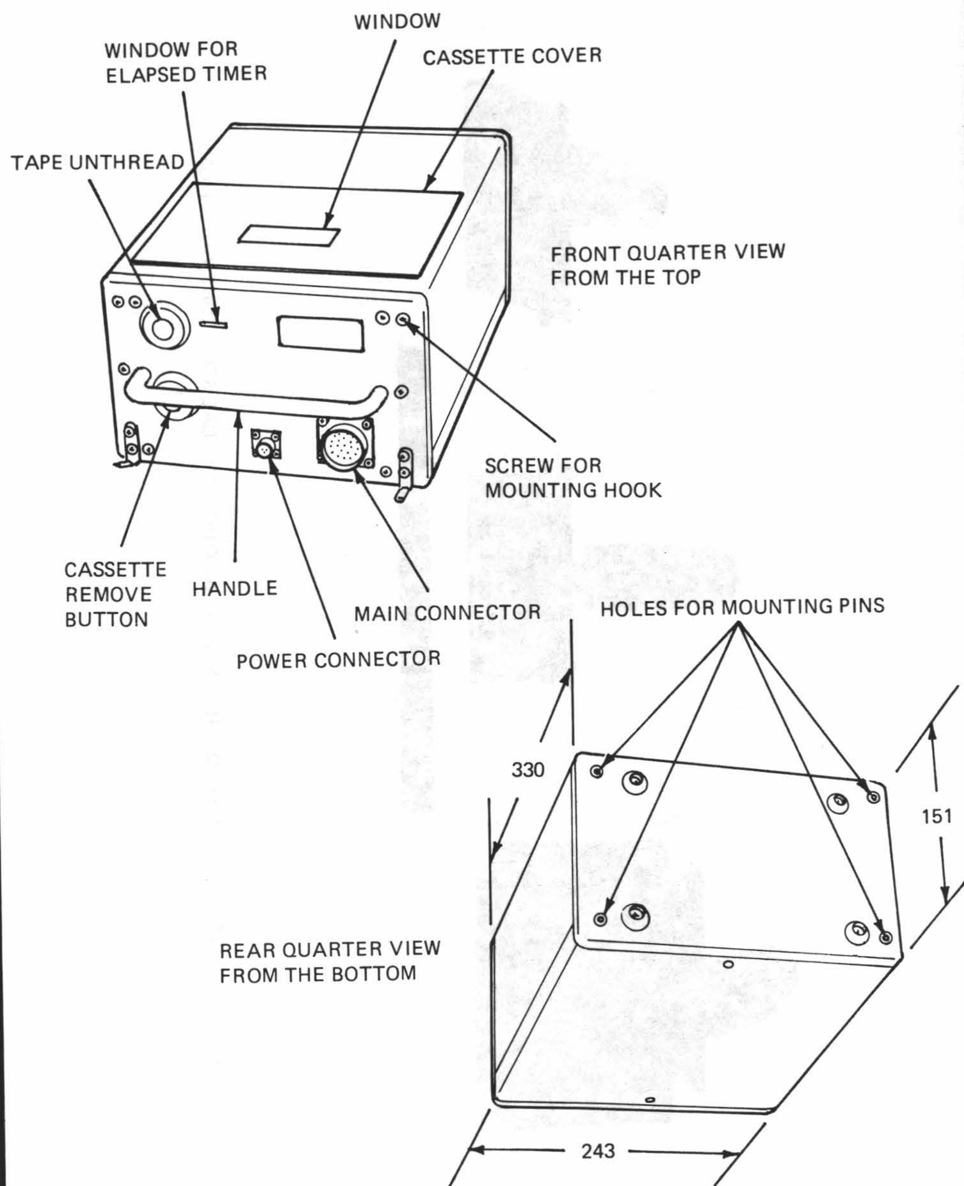


FIGURE 9. AVTR MECHANICAL OUTLINE

SUPPORT EQUIPMENT

The CTVS Functional Test Set shown in Figure 10 is used for intermediate level testing of the CTVS. It has been designed for functional testing of the complete CTVS camera, or the VSH alone. A light box and collimator, shown along side the test console, is used for focusing the CTVS, and includes test targets with variable brightness up to 500 ft. candles.

SUMMARY

The Cockpit Television Sensor System is a versatile and rugged one which can expand the effectiveness of operational and training missions by providing instant post flight evaluation, plus the option of a real time display for two seat aircraft. The very small size of the Video Sensor Head, and its versatile construction, make it a candidate for many applications in addition to recording the HUD. The addition of a split screen control unit effectively doubles the capability of the AVTR with a modest trade off in horizontal resolution. The CTVS camera and AVTR have been flight tested, and are currently in use, on a variety of USAF and USN aircraft.

ACKNOWLEDGEMENT

The final development of the CTVS camera was accomplished under contract number F33657-78-C-0484 from ASD, Wright Patterson Air Force Base, and contributions by many people at ASD are gratefully acknowledged. Credit for the initial concept and early development of the CTVS which was called the Electronic Gunsight Camera in 1976, must be shared with members of Tactical Air Command and the Air Force Avionics Laboratory without whom the development of this system might never have been initiated.

REFERENCES:

1. Bashe, R. and Balopole, H.L., ''Electronic Gunsight Camera'' Air-to-Air Fire Control Review, AF Academy, Colorado, October 1976.
2. Hoagland, K.A. and Balopole, H.L. "CCD TV Cameras, Utilizing Interline-Transfer Area Image Sensors", Proc of the 1975 International Symposium on the applications of CCD, San Diego, Cal., October 1975.

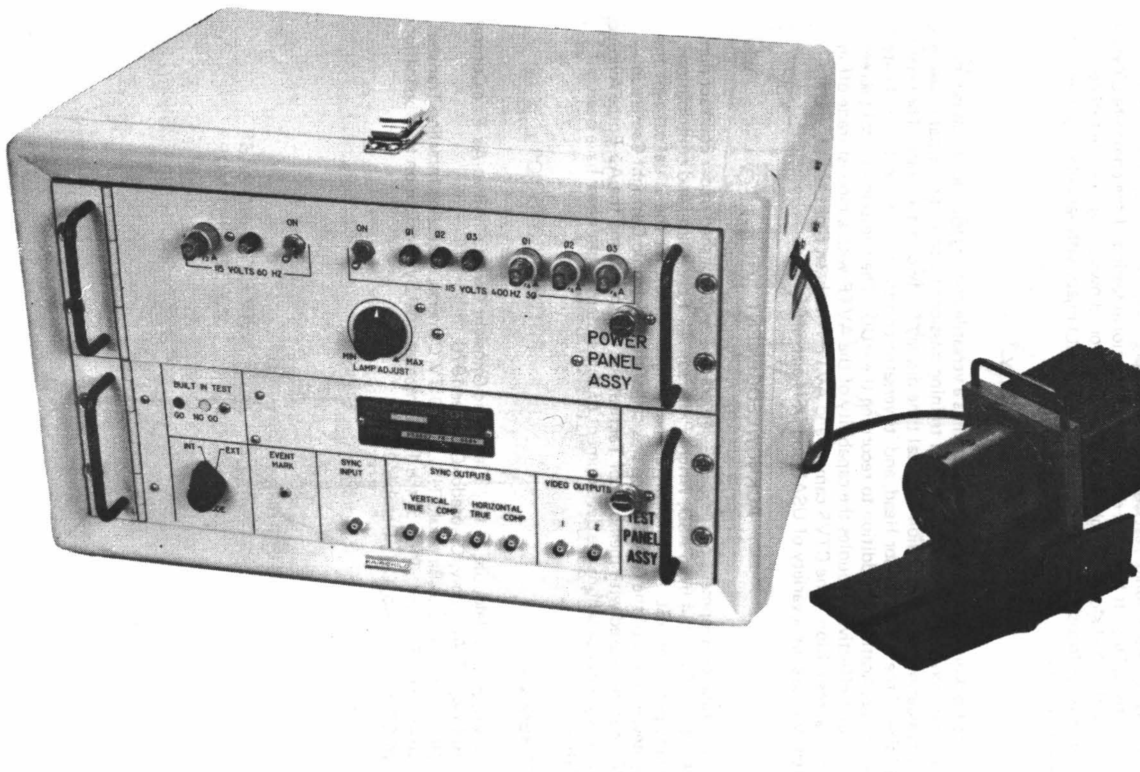


FIGURE 10. CTVS FUNCTIONAL TEST SET

APPENDIX A – CTVS QUALIFICATION TEST LEVELS

TEST	SPECIFICATION/ PARAGRAPH	TEST LIMITS
Explosive Atmosphere	MIL-STD-810C Method 511.1 Proc. I	Sea Level to 30,000 ft. at temperatures up to 71°C with CTVS operating
Shock (Crash Safety)	MIL-STD-810C Method 516.2 Proc. III	40 g, 11ms duration, 1/2 Sine 2 shocks in each direction (12)
Humidity	MIL-STD-810C Method 507.1 Proc I	71° at 95% RH for 6 hours, decreasing to 30°C at > 85% RH in the next 16 hours 240 hours total
Solar Radiation	MIL-STD-810C Method 505.1 Proc I & Item Specification	1135 Watts/m2 at an ambient of 71°C for six (6), eight (8) hour cycles.
Explosive Decompression	ASD/ENAM-77-23	Air pressure change from 11.1 psia to 0.65 psia in less than .035 seconds
Sun Exposure to Sensor	ASD/ENAM-77-23	1135 Watts/m2 for 50 seconds with camera operational 1135 Watts/m2 for periods > 1 hour with camera operational
Salt Fog	MIL-STD-810C Method 509.1 Proc I	96 hours at 35°C 5% Salt Solution
Rain	MIL-STD-810C	2-5 inches per hour with 40 mph winds for four (4) 30 minute periods.
Fungus	Certification	Parts selection review for fungus non-nutrient
Dust (fine sand)	MIL-STD-810C Method 510.1 Proc I	Dust concentration of .3 grams per cubic ft. with air velocity up to 1,750 fpm for 22 hours
Temperature/Altitude	MIL-STD-810C Method 504.1 Cat 4	-62°C to 95°C storage -54°C to 55°C operating to 30,000 ft. 71°C intermittent operation
Sine Vibration	ASD/ENAM-77-23	7 g endurance level 1 hours/axis 6 g performance level 1 hour/axis
Radiation Vibration	ASD/ENAM-77-23	9.5 g rms endurance level 1/2 hour/axis 5.14 g rms performance level 2 hours/axis
Gunfire Vibration	ASD/ENAM-77-23	Up to 3 g sine vibration with random vibration background of 4.17 grms for 1 hour/axis

APPENDIX A – CTVS QUALIFICATION TEST LEVELS (CONTINUED)

TEST	SPECIFICATION/ PARAGRAPH	TEST LIMITS
Gunfire Vibration	ASD/ENAM-77-23	Up to 5 g sine vibration with random vibration background of 4.86 grms for 1 hour/axis
Reliability Demonstration	MIL-STD-781C TEST PLAN XIVC for fighter aircraft	Combined environment cycle of thermal, vibration humidity, and input voltage designed to simulate a typical aircraft mission. Eight cameras were tested for a total of 3902.4 hours
Conducted Emissions, Power Leads	MIL-STD-462, Notice 2 Test Method CE03	MIL-STD-461A, Notice 3, Paragraph 6.2, 20 kHz to 50 MHz, narrowband and broadband emissions.
Conducted Emissions, Control & Signal Leads	MIL-STD-462, Notice 2 Test Method CE04	MIL-STD-461, Notice 3, Paragraph 6.2, 20 kHz to 50 MHz, narrowband and broadband emissions.
Conducted Susceptibility Power Leads	MIL-STD-462, Notice 2 Test Methods CS01, CS02 and CS06	MIL-STD-461, Notice 3, Paragraphs: 6.4 – 30 Hz to 50 kHz, narrowband susceptibility 6.5 – 50 kHz to 400 MHz, narrowband susceptibility 6.6 – 1 to 10 PPS, Spike susceptibility
Radiated Emissions	MIL-STD-462, Notice 2 Test Method RE02	MIL-STD-461, Notice 3, Paragraph 6.12, 14 kHz to 1 GHz, Broadband emissions and 14 kHz to 10 GHz, Narrowband emissions.
Radiated Susceptibility	MIL-STD-462, Notice 2 Test Methods RS02 and RS03	MIL-STD-461, Notice 3, Paragraph 3: 6.18a – Twenty Amperes 400 Hz susceptibility 6.18b – 100 PPS, Spike susceptibility 6.19 – 14 kHz to 10 GHz Narrowband susceptibility
Electromagnetic Compatibility Systems	MIL-E-6051D	Aircraft installed Electromagnetic Compatibility A10 Aircraft, F4 Aircraft, F15 Aircraft, F16 Aircraft

UNITED KINGDOM

SALES OFFICES

Fairchild Camera & Instrument (UK) Ltd.
230 High Street
Potters Bar
Hertfordshire EN6 5BU England
Tel: Potters Bar (0707) 51111
Telex: 262835

Fairchild Camera & Instrument (UK) Ltd.
17 Victoria Street
Craigshill
Livingston
West Lothian EH54 5BG Scotland
Tel: Livingston (0506) 32891
Telex: 72629

DISTRIBUTORS

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Sussex RH13 5PX
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Reading
Berkshire RG3 1DZ
Tel: Reading (0734) 585171
Telex: 848370

Comway Electronics Ltd.
Market Street
Bracknell
Berkshire RG12 1QP
Tel: Bracknell (0344) 24765
Telex: 847201

ITT Electronic Services
Edinburgh Way
Harlow
Essex CM20 2DF
Tel: Harlow (0279) 26777
Telex: 81525

Jermyn-Mogul
Vestry Estate
Sevenoaks
Kent TN14 5EU
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Telex: 95142

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Oldham
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Telex: 669619

Macro Marketing Ltd.
Burnham Lane
Slough
Berkshire SL1 6LN
Tel: Burnham (06286) 4422
Telex: 847945

SCANDINAVIA

SALES OFFICE

Fairchild Semiconductor AB
Svartensgatan 6
S-11620 Stockholm
Sweden
Tel: 46/8/449255
Telex: 854-17759

DISTRIBUTORS

Datamatik A/S
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Oslo 10
Norway
Tel: 00947/230173O
Telex: 16967

E. Friis Mikkelsen AS
51 Krogshojvej
DK2880 Bagsvaerd
Denmark
Tel: (02) 986333
Telex: 37350

ITT Multikomponent
Box 1330
S-17125 Solna
Sweden
Tel: 00946/8830020
Telex: 10516

Multikomponent
Kuortaneenkatu 1
SF-00520 Helsinki 52
Finland
Tel: 009358/0739100
Telex: 121450

Multikomponent (Standard Electric) AS
Fabriksparken 31
DK 2600 Glostrup
Denmark
Tel: (02) 456645
Telex: 33355

Norqvist & Berg
Box 9145
S-10272 Stockholm
Sweden
Tel: 00946/8690400
Telex: 10407

FAIRCHILD
A Schlumberger Company

FAIRCHILD Camera & Instrument (UK) Ltd.
230 High Street, Potters Bar, Hertfordshire EN6 5BU England
Tel: Potters Bar (0707) 51111, Telex: 262835

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